FINAL REPORT

PHASE C

Thin-Film Personal Communications and Telemetry System (TFPCTS)

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MELPAR, INC.
7700 Arlington Boulevard
Falls Church, Virginia 22046

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FINAL REPORT ON RESEARCH, DEVELOPMENT, DESIGN, INTEGRATION AND TESTING OF THIN FILM PERSONAL COMMUNICATIONS AND TELEMETRY SYSTEM (TFPCTS)

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Submitted to

National Aeronautics and Space Administration
Manned Spacecraft Center
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Submitted by

Melpar, Inc.
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October 1968

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1. INTRODUCTION

This final report is submitted in compliance with the terms of Contract NAS 9-3924 and reports on all work performed on the contract between 21 December 1964 and 13 August 1968. By the terms of the contract, the technical effort was divided into three separate, distinct phases. The first phase (Phase A) consisted of a research program of applicable device materials and the development of an ultra-high frequency, thin film device. Phase B consisted of the fabrication of function circuit blocks with the development device (from Phase A) and existing thin film devices to produce a Thin Film Personal Communications and Telemetry System (TFPCTS). Phase C was to integrate the functional blocks into an operating and tested system.

The technical efforts on Phases A and B have been described in detail in the final reports for each phase previously submitted. However, the results and conclusions of these phases are briefly summarized in the following sections. The technical efforts on Phase C are discussed in much greater detail since this is the final report on that phase and on the contract.

The last section of this report provides a brief presentation of a new phase of the program which Melpar feels should be funded to produce a fully operable system for NASA use.

2. PHASE A - RESEARCH PHASE

Phase A consisted of a research program of device materials and the development of an ultra-high frequency, thin film device for use in the TFPCTS to be designed in Phase B. In the first quarter of Phase A, the "High Frequency Substrate Investigation" was completed, and substrates and capacitors were determined to be very satisfactory in performance beyond the required 300 mc.

In the third quarter, the "Inductor Investigation" and "High Magnetic Permeability Films" research efforts were concluded. Both of these investigations had been extended in both time and manpower to ensure that sufficient knowledge was obtained to properly evaluate their potential use in the TFPCTS. The inductors were developed to a point where they seemed practical and were included with the other passive components as available for use in the design phase. Ferrite films were formed in vacuo, using standard vacuum deposition techniques for the first time under this contract. However, further development, beyond the scope of this contract, is necessary before this thin-film material can be optimized for circuit use. The chemical ferrite formed was reported in a NASA New Technology Brief.

One of the most exciting areas of research was the "Metal Base Transistor." Early in the program a thin-film diode operating through the Schottky barrier mechanism for rectification was fabricated. This metal-semiconductor junction was so much better than the previously used thin-film diodes of the metal-dielectric-semiconductor barrier type that it was scheduled as the diode and varactor devices

for this program. The metal-semiconductor junction also appeared promising for high-frequency performance. A NASA New Technology Brief was submitted on this development. The metal base transistor and the diode were worked on concurrently. The formation of the diodes was very susceptible to the purity and present impurities of the semiconductors, and a great amount of effort has been expended in semiconductor evaluation. Before the close of this phase, however, some transistor action was obtained in a few transistors formed from these diodes.

"High-Frequency Thin-Film Triodes" was considered one of the most difficult research and development areas of the program. Special geometric configurations were dev eloped for high-frequency TFT's. New methods for completing the devices with the narrowest possible gates were evolved. Special attention was given to selecting new semiconductor materials and optimizing both the new and the standard TFT semiconductor materials. The results at the end of this phase were that the TFT's had been improved an order of magnitude from 1 to 2 mc to 30 mc.

During Phase A, Melpar has supported a parallel effort to develop the circuits required to initiate Phase B. The listing below gives the estimate of the number of circuits which can be completely fabricated in thin-film form.

The circuits that were breadboarded in discrete form included:

a. VCO's.

b. VCO filters.

c. Audio amplifiers.

d. I-F amplifiers.

e. R-F amplifiers.

f. R-F oscillators.

g. Frequency multipliers.

h. Mixers.

In all cases the circuits were designed with components that it was hoped have similar characteristics to thin-film components. The breadboard was designed in modular form so that thin-film substrates can be substituted for the discrete component modules.

Reports on the circuit layout and performance are part of the Phase B effort. Except for the transmitter output power, the circuits of the breadboard met desired characteristics of the contract work statement. The output power could not be attained at that time with field effect transistors.

A second problem area was the receiver input for large signals. The TFPCTS required that the receiver should be capable of operation at a 1.4-volt peak-to-peak input signal. At this level the r-f amplifier is saturated and introduces considerable distortion. This situation can be corrected by using AGC voltage to tune the input slightly off the center frequency. Since the transistor input capacitance is a function of the applied voltage, the AGC voltage can be applied to the gate in a conventional manner.

COMPONENT ESTIMATES FOR TFPCTS

	Transistors	Coils	R	C	Diodes	Other
Duplex transmitter	4 (HF)	5	5	14	-	1 crystal
VCO's (7)	14 (LF)		42	14	14	-
VCO filters	-	-	18	18	-	-
VCO adder amplifier	2 (LF)	-	8	2	-	-
2.3-kc filter	2 (LF)	-	5	5	-	-
VOX duplex	6 (LF)	-	18	6	1	-
Duplex receiver	4 (HF)	5	5	14	-	1
Simplex receiver	4 (HP)	5	5	14	-	1
Diplexer	-	5	5	-	-	-
I-F duplex	15 (LF)	-	45	28	3	-
I-F simplex	15 (LF)	-	45	28	3	-
Audio duplex	4 (LF)	-	12	9	-	-
Audio simplex	4 (LF)	-	12	9	-	-
Simplex transmitter	4 (HF)	5	5	14	-	1
2.3-kc filter	2 (LF)	-	5	5	-	-
VOX simplex	6 (LF)	-	18	6	1	-
Power supply	4 (High current)	-	15	10	4	-
	6 (Low power)				1 reference	
VCO regulators					7 reference	
Totals	16 HF 76 LF	25	268	196	26 diodes	4
	4 high current	(2 large C)			8 reference	

At the end of the research phase (Phase A), the desired thin film active device for ultra-high frequency operation had not been successfully produced. However, the research improved the TFT and indicated that higher frequencies than those achieved (30 mc) were possible. A discrete breadboard of the TFPCTS, designed to utilize these TFT's if they could be further improved, operated to the desired level for most characteristics, and NASA approved this concept and authorized Phases B and C to introduce thin film modules for the discrete functions of the breadboard design.

3. PHASE B - DESIGN PHASE

It was originally intended that Phase B would involve designing the TFPCTS for thin film form utilizing the ultra-high frequency, thin film active device developed in Phase A. However, this was changed to accommodate the actual results achieved in Phase A. As approved for initiation by NASA, Phase B actually involved substituting thin-film components for the discrete components and modularizing the breadboard TFPCTS produced by a separate Melpar effort during Phase A. Because of the promise of the TFT at the end of Phase A and the planned continued efforts to produce further improvements as a Melpar supported program, the modules were to utilize field effect transistors. It was thought that the TFT's could be readily substituted for these transistors in the modules.

Three results from Phase B seemed to offer promise to the general electronics community. First was the development of a universal VHF thin-film circuit module which was used in all the VHF circuits, including such diverse functions as the modulator and power amplifier. This could be the introduction into a very inexpensive system fabrication method.

Second: The first IF module and the second IF module were probably the most complex in total thin-film resistor and capacitor component count ever attempted. For example, the second IF module is 1 x 3 inches in size and contains a frequency selective IF strip, its own AGC and an audio detector and amplifier. This involves

42 thin-film resistors and 28 thin-film capacitors on each substrate. Of course, it was not the total number of resistors or capacitors that was of significance, but the fact that this large resistor-capacitor total was attempted on an individual substrate. The attainment of any appreciable yields for this completely vacuum deposited thin-film circuit would be a breakthrough in the state-of-the-art.

Third: The thin-film voltage controlled oscillators fabricated for this contract had exceptional linearity with a wide frequency range over a voltage input span the equivalent of the B+ supply.

There were two major problem areas in Phase B. The module or substrate packaging techniques and the stability of the TFT's. As described in this previous report, a suitable packaging process which protects the substrates without affecting the electrical performance of the circuits was evolved. Steps were made in defining TFT stability problems and methods of stabilization were tried. Most of the circuits were designed using field effect transistors so that any breakthrough in achieving TFT stability would permit their use in the TFPCTS.

Since the overall system design and the individual module design are intertwined with the system fabrication, they are presented in detail in the sections on Phase C.

4. PHASE C - INTEGRATION AND TEST PHASE

Phase C involved the integration of the independent modules designed in Phase B into an operating and tested TFPCTS and the delivery of two units. The results of this phase are presented in relation to the telemetry unit, the dual transmitter, the dual receiver, and the rf portion.

Detailed procedure for thin film processing and circuit assembly are presented in Appendix "A" and were used to fabricate all modules making up the system discussed below.

Photographs of the system package are shown in Figures 1, 2, and 3. An assembly drawing of the system is shown in Sketch 1 and a wiring (block) diagram is shown in Figure 4. The major parts of the system are the telemetry unit, the dual transmitter, the dual receiver, the dual diplexer, the dc power supply, the mode switch, the coaxial relay, and the mother P.C. board. Minor parts include the multiple pin connector for dc and audio frequency signals, the coaxial antenna connector, a 20K ohm potentiometer used for volume control for the two receivers, a mounting clamp and shim for the coax relay, and the case, bracket, and cover which form the package enclosure.

The weight and volume of each delivered system is 18.44 ounces and 24.7 cubic inches. Design objectives (target values) were 10 ounces and 10 cubic inches.

4.1 Telemetry Unit

The function of the telemetry unit is to convert seven dc or slowly varying voltages to constant amplitude ac voltages in which

the frequency represents both the origin and magnitude of the input signal. The telemetry unit consists of 7 voltage controlled oscillators (VCO's); 3 double twin T filters; a substrate containing 2 source followers, 7 summing resistors, and a coupling capacitor; and an operational amplifier. The wiring diagram for the telemetry unit (similar to a block diagram) is shown in Figure 5. The schematic diagrams and substrates for the telemetry unit modules are shown in Figures 9 through 16. The twelve substrates comprising the telemetry unit are mounted together on the mother board at one corner of the system package as indicated in sketches 1 and 5.

Each VCO employs a multivibrator circuit to produce an approximate square wave output having a constant magnitude of about 7 volts P-P and a frequency equal to the specified center frequency when the input equals +2.5 Vdc. The output frequency varies linearly with the input voltage, which ranges from 0 to +5 Vdc. The center frequencies and the variation in frequency (bandwidth deviation) as the input varies ±2.5 volts from its midrange value of +2.5 volts are: 4 KHz ± 5%, 5.4 KHz ± 5%, 6.8 KHz ± 5%, 8.2 KHz ± 5%, 9.6 KHz ± 4%, 11.0 KHz ± 3%, and 12.4 KHz ± 3%.

The room temperature tolerance, although not clearly specified, is interpreted to be ± 1% of the bandwidth over the entire frequency range. For example, the output frequency of the 4 KHz VCO, with a bandwidth of 400 Hz, should be within ± 4 Hz of the ideal frequency as the input varies from 0 to 5 Vdc at 25°C. (The ± 1% figure is listed as "bandwidth linearity.")

The temperature stability, stated as a percentage of the "total deviated bandwidth," is interpreted to mean the frequency may vary from its room temperature value by the stated percentage of the bandwidth as temperature varies ± 25°C from + 25°C and where the input voltage is held constant anywhere within its 0 to +5 volt range. For example, the frequency of the 4 KHz VCO may vary ± 2% of 400 Hz or ± 8 Hz from its actual 25°C value, which should be within ± 4 Hz of the ideal 25°C value. The listed temperature stability percentages are ± 2% for the four lowest frequencies, ± 10% for the highest frequency, and ± 5% for the remaining two frequencies.

The desired frequency response of 2 cps for all channels except for the highest frequency channel, for which 30 cps is listed, is interpreted to mean that the output frequency of each channel should remain constant for a sinusoidal input voltage of fixed amplitude and variable frequency ranging from zero to the stated "frequency response." This was probably included to minimize dynamic errors in the transmission of rapidly changing data.

The outputs of the two lowest frequency VCO's are filtered to prevent higher harmonics of these channels from being transmitted. If this were to occur, the harmonics would be indistinguishable from some of the higher frequency data channels and the transmitted data would be erroneous. The filtering is accomplished by double twin T filters which are tuned to block the harmonics. The output of the 4 KHz VCO is fed through two filters tuned at 8 and 12 KHz to block

the second and third harmonics. The output of the 5.4 KHz VCO is fed through a filter tuned at 10.8 KHz to block the second harmonic. The filters are designed to reject all harmonics over the frequency range of the VCO. For example, the 8 KHz filter rejects 8 KHz ± 5% since the fundamental is 4 KHz ± 5%. Other harmonics lie beyond the range of the highest frequency channel.

A typical pair of filters for the 4 KHz VCO attenuate the fundamental 44 db, the second harmonic 77 db, and the third harmonic 85 db. A typical filter for the 5.4 KHz VCO attenuates the fundamental by 28 db and the second harmonic about 60 db. Thus the harmonics are attenuated at least 30 db more than the fundamental.

It is noted that a perfect square wave does not contain even harmonics, but the output wave shapes of the VCO's are somewhat distorted and therefore contain second harmonics. It was thus considered necessary to provide for filtering of second harmonics.

The seven telemetry signals are ultimately fed into the audio input of the modulator of the duplex transmitter. The signals should have approximately equal amplitudes so that the transmitted signals are of equal strength.

Another characteristic of the telemetry unit is that harmonics above the highest frequency channel are filtered out, as well as harmonics within range of the seven channels. This is desirable because a non-linear receiver could sense signals having frequencies equal to the difference in the frequencies of two harmonics. The

"difference frequencies" may be within the bandwidth of one or more data channels and thus result in ambiguity.

Both of the above features are satisfied by means of an operational summing amplifier with a parallel RC network in the feedback loop.

The amplifier is contained on one substrate (Figures 15 and 16), and the summing resistors, coupling capacitor, and two source followers are contained on an adjacent substrate (Figures 13 and 14). The source followers are required for the two lowest frequency channels to minimize loading of the twin T filters, which have high output impedance. The value of resistance and capacitance in the feedback network is such that the harmonics of the five highest frequency channels are filtered out. The output of the operational amplifier for each channel is equal to the input voltage multiplied by the ratio of feedback impedance to input (summing) resistance for the channel. The total output of the amplifier is the sum of the output voltages for the seven channels. The values of the summing resistors are such that, in conjunction with the input voltage and feedback impedance for each channel, the output for each channel is about 0.5 volts, P-P $\pm$ 20%.

The open loop gain of the operational amplifier is at least 1000 volts/volt over the frequency range from 3.8 to 12.8 KHz. The feedback impedance is approximately $R_1/(1 + R_1C_1S) = R_1/(1 + j\omega R_1C_1)$, where R_1 = 290 kilohms and C_1 = 325 pf nominal. The original nominal design values were 410 kilohms and 220 pf. The change resulted from

an error in the capacitor area in the mask design. It was decided to leave R_1 at its untrimmed value, 290 K, so that the RC time constant would be the same as in the original design. Thus, the feedback impedance is about 30% lower, at all frequencies, from the original design values. This is compensated for by reducing all the summing resistors by 30% from their original design values. This was accomplished by depositing the resistors to values 15% below the original values and by trimming only the summing resistors for the two lowest frequency channels, R1 and R2. It was necessary to trim R1 by cutting away a portion of the rhenium, in addition to opening the shortening bar, due to an error in the mask design.

The drain to gate resistors for the source followers and the operational amplifier, stages (a) and (b), were cut out of the circuits due to a change to 2N3071 transistors which operate best at zero bias; the original transistors required a positive bias. For the source followers, the gate to source resistors are no longer critical and are left at their untrimmed values. The load resistors, (source to ground), for the source followers are trimmed to obtain a source voltage of about +5 Vdc, or half the supply voltage.

The gate to ground resistors for the operational amplifier were reduced below their original design values in order to reduce the amplifier gain to 1000 volts/volt $\pm \frac{5}{0}$ % to prevent instability after closing the feedback loop. It was often necessary to jumper the larger non-trimmable segments of the resistors with wire and use smaller trimmable resistor segments in order to reduce the resistors

sufficiently. The instability problem probably resulted from the reduction of resistor R1 in the feedback network which increased the gain of the feedback network.

Because of the high precision required of the Twin T filters and VCO's, special trimming procedures are required. Resistors must be increased in increments as low as .06%, therefore it is generally necessary to reduce the resistor width by cutting out portions of the rhenium, as well as opening shorting bars. These procedures are listed below:

a. Double Twin T Filter Procedure

1. Measure and record all capacitors.
2. Calculate required resistor values.
3. Trim resistors within ± 1% of calculated values.
4. Determine the attenuation at fundamental and harmonic bandwidths (frequency response test). Attenuation shall be no greater than 30 db within fundamental bandwidth; attenuation shall be at least 30 db greater within harmonic bandwidth.

Equations

$$R_1 = R_2 \qquad R_4 = R_5$$

$$R_1R_2 = \frac{C_1 + C_2}{C_1C_2C_3\omega_1^2} \qquad R_4R_5 = \frac{C_4 + C_5}{C_4C_5C_6\omega_2^2}$$

$$R_3 = \frac{1}{(R_1 + R_2)\ C_1C_2\omega_1^2} \qquad R_6 = \frac{1}{(R_4 + R_5)\ C_4C_5\omega_2^2}$$

$$\omega_1 = 2\pi f_1 \qquad \omega_2 = 2\pi f_2$$

where

R = ohms

ω = rad/sec

C = farads

f = cycles/sec

f_1 = min. frequency in harmonic band

f_2 = max. frequency in harmonic band

b. VCO Procedure

1. Frequency is approximately proportional to the reciprocal of $(R_{2a}C_a + R_{2b}C_b)$. The two RC products must be equal in order to produce a symmetrical wave shape. In order to facilitate trimming of R_{2a} and R_{2b}, trim C_{2a} and C_{2b} to the following values: 900 pf for the 4 KHz VCO, 600 pf for the 5.4 and 6.8 KHz VCO; and 300 pf for the remaining four VCO's.

2. Trim R_1 to 10 kilohms $\pm$ 15%.

3. Increase R_{2a} to the approximate value of R_{2b} by removing shorting bars.

4. Trim the load resistors, R_{1a} and R_{1b}, to 47 K $\pm$ 40%.

5. Measure and record all resistors and capacitors.

6. Connect transistors, diodes, and terminal pins.

7. Connect the VCO into a functional test setup with regulated dc supplies for +10 and +3 Vdc $\pm$ .05% and with the actual load to be used. The load consists of twin-T-filter substrates (if required), the source follower, summing resistor, and coupling capacitor substrate, and the operational amplifier substrate. It is

not necessary to connect the other VCO's since they do not load one another. The input consists of an adjustable 0 to +5 Vdc supply. The VCO output is measured with a high input impedance frequency counter and oscilloscope. Dc voltages are measured with a dc fluke meter to an accuracy of ± .01%.

8. Record the dc voltage, V, at test point TP 1 and the frequency, f, of the output signal for 0 and +5 Vdc inputs.

9. Trim R_2 to the following value within ± 5%.

$$R_2 = .9\ R_1 \left(\frac{1}{1.2}\ \frac{f_1\ \text{des}}{f_1\ \text{act}}\ \times\ \frac{\Delta f\ \text{act}}{\Delta f\ \text{des}}\ \times\ \frac{\Delta V\ \text{in}}{\Delta V\ \text{act}} - 1\right)$$

where

f_1 = output frequency when input = 0 Vdc

f_2 = output frequency when input = +5 Vdc

$\Delta f = f_2 - f_1$ = bandwidth

V_1 = voltage at TP 1 when input = 0

V_2 = voltage at TP 1 when input = +5 Vdc

$\Delta V = V_2 - V_1$

ΔV in. = input voltage range = 5 Vdc

act. = actual value

des. = design or desired value

10. Set input at 0 Vdc and reduce frequency to 5% above its correct design value by increasing R_{2a} and R_{2b}. Increase R_{2a} and R_{2b} in small alternate steps so that the positive and negative portions of the output wave are symmetrical, i.e., have equal pulse widths.

11. Reduce bandwidth, Δf, to its correct value $^{+2}_{-0}$ % by increasing R_2.

12. Reduce f_1 to its correct value ± the specified room temperature tolerance, by further increases in R_{2a} and R_{2b}.

13. Reduce Δf to its correct value ± the specified room temperature tolerance, by a further increase in R_2.

14. Repeat step 12, if necessary.

4.2 Dual Transmitter

The dual transmitter consists of two VHF/AM transmitters mounted on a common printed circuit board. One transmitter termed "duplex" transmits both voice and telemetry signals simultaneously; the other transmitter termed "simplex" transmits a voice signal only.

When one transmitter is operating, the other is turned off. The reason for including a simplex transmitter in the system was probably for greater reliability. If the duplex transmitter fails, or if its voice signal is too weak, the simplex transmitter, with its stronger voice modulation, may be used.

The simplex transmitter differs from the duplex transmitter in three other respects as follows:

a. The simplex transmitter contains a voice operated switch (VOX) which cuts off the RF output of the modulator and thereby reduces power consumption to a low level when a voice signal is not present. The switch has an attack time of 0.1 millisecond and a drop-out time of 2 seconds.

b. The simplex transmitter is required to transmit audio signals within the frequency range of 0.25 to 2.3 KHz, compared to 0.25 to 14 KHz for the duplex transmitter.

c. A voice signal of 1 mV rms at the microphone output, referenced to 1 KHz, causes the rf carrier to be amplitude modulated to a level of 95% in the simplex transmitter, but only 20% in the duplex transmitter. In the duplex transmitter, the seven telemetry signals produce a modulation level of 75%, therefore, the total modulation level is 95%, including voice.

In all other respects, the two transmitters are the same. Carrier frequency is 296.8 mHz ± .005%. Average, unmodulated output carrier power should be no less than 150 milliwatts when measured at the antenna terminal. The voltage standing wave ratio of the load is between 1:1 and 2:1 when referenced to 50 ohms. Linearity should be within 5% of the best single straight line. Modulation response should be flat within ± 1.5 db over the specified audio frequency range. The voice signal is attenuated at 24 db/octave above 2.3 KHz. Voice input impedance is 10 kilohms at 1 KHz. Modulation symmetry should be such that the positive and negative modulation indexes are equal within 10% under all conditions of modulation. Incidental frequency modulation should not result in a deviation of the carrier output frequency greater than 1 KHz. The carrier power level should not shift more than 5% when modulated. Spurious and harmonic radiation should be least 40 db below the unmodulated carrier level.

Each transmitter consists of a shielded RF section and an unshielded AF section (see Figure 6 and Sketch 8). The RF section, housed in a grounded brass container, consists of a 296.8 mHz oscillator, a modulator, a driver amplifier, and a power amplifier. The 296.8 mHz oscillator consists of a 98.9333 mHz oscillator, a tripler, and two amplifiers (called tripler amplifiers No. 1 and No. 2). See Figures 27 through 30 and Sketches 8a and 8b.

The audio section consists of an audio amplifier substrate, a substrate containing a voice filter, a voltage divider for the modulator bias, and summing resistors for voice and telemetry unit signals; and, for the simplex transmitter, a VOX substrate. See Figures 17 through 22.

4.2.1 Audio Amplifier

The audio amplifier, shown in Figures 17 and 18, contain three stages of amplification. There are provisions for applying a positive or negative bias to the three stages, with individual bias adjustment at each stage (see resistors R2, R4, R6, and R8). The transistor presently used is the Amelco 3071 FET junction transistor which operates best at zero bias; therefore, terminal 5 is grounded, resistor R8 is not required, and the trimmable portions of resistors R2 and R4 are not required. The characteristics of the audio amplifier are:

Input Impedance	10 k ohms
Frequency Response	250 Hz to 2.3 KHz
Gain	200 to 2500 selectable

Undistorted Output Swing	5V peak-to-peak
Output Impedance	10 K ohms max.

This circuit receives its signal from the voice microphone and is required to produce a signal that will modulate the transmitter to a 95% level for the simplex transmitter and a 20% level for the duplex transmitter with a 1 millivolt rms signal, referenced to 1 KHz, from the microphone. Since a 1 volt rms signal is sufficient to drive the modulation to 95%, the gain must be 1000 v/v and about 575 v/v for the simplex and duplex transmitters, respectively. (The voice filter has unity gain out to its "roll off" frequency.)

The audio amplifier assembly procedure is as follows:

1. Trim the input resistor, R1, to 10 K ohms.

2. Connect the transistors and terminal pins.

3. For the simplex transmitter, apply +10 Vdc to terminal 10, ground terminals 5 and 6 and apply a 1 mV rms, 1 KHz input signal from a signal generator having a 10 K ohm output impedance (to simulate the microphone impedance). Load the audio amplifier with the low pass, voice filter.

4. Increase the gain by increasing the load resistors, R3, R5, and R7, until the output of the voice filter equals 1 volt, rms.

5. For the duplex transmitter, the audio amplifier gain must be adjusted as a function of the telemetry output voltage and the summing resistors, R7 and R8, located on the voice filter substrate.

   a. Trim R7 to the following value:

$$R7 = \left(\frac{0.79}{V} - 1\right) R8$$

where V = telemetry unit output in volts rms, with all telemetry unit inputs set at +2.5 Vdc.

b. Using the test setup of Step 3, increase the gain of the audio amplifier until the output of the voice filter equals the following voltage, V. (The telemetry unit must be disconnected.)

$$V = 0.21 \left(1 + \frac{R8}{R7}\right)$$

This should result in a 20% modulation by the voice signal and 75% modulation by the seven telemetry signals.

4.2.2 Low Pass, Voice Filter

The low pass voice filter consists of two Butterworth filters used in cascade (see Figures 19 and 20). Each filter has a break frequency of 2.3 KHz with an attenuation of 12 db per octave beyond the break frequency. Since the overall transfer function is the product of the transfer functions of the two filters, the net attenuation beyond 2.3 KHz is 24 db/octave.

The assembly, trimming, and test procedure is listed below:

a. Measure C1 through C4 and then trim R1 through R4 to the following values.

$$R_1 R_2 = \left(\frac{1}{\omega^2 C_1 C_2}\right) \qquad R_1 \simeq R_2$$

$$R_3 R_4 = \left(\frac{1}{\omega^2 C_3 C_4}\right) \qquad R_3 \simeq R_4$$

where $\omega = 2\pi f = 2\pi \times 2300 = 14{,}430$ rad/sec

R = ohms

C = farads

b. Connect the two transistors and terminal pins into the circuit.

c. Apply +10 Vdc to pin 4 and ground pin 6.

d. **Trim the source follower load resistors, R5 and R6, so** that the drain voltage at Q1 and Q2 is 5 ± 1 Vdc.

e. Perform a frequency response test from 0.25 to 14 KHz **with a 1 volt rms input. The gain should equal one from 0.25 to** approximately 2.3 KHz and shall attenuate at a rate of 24 db/octave beyond 2.3 KHz.

4.2.3 Summing Resistors for VOX and Modulator Bias

Summing resistors are required to add the VOX output voltage to the output of the voltage divider, R10, in order to supply proper biases to the modulator during "on" and "off" conditions for the simplex transmitter. Resistor R9 on the voice filter substrate satisfies this requirement for the voltage divider. In debugging, it was determined that an additional summing resistor is required for the VOX signal, and a discrete resistor was added.

Modulators require a bias of -1.9 to -2.9 Vdc when operating. The exact voltage is unique for each transmitter and is determined when the RF portion of each transmitter has been assembled. (See Note 7 for the RF schematics.)

For simplex transmitters, the discrete summing resistor, R, is selected so that R = 1.539 x R9, the output of this resistor and the filter substrate are connected to the modulator load, the VOX output, when in the "on" condition (+8 Vdc), is applied to the input

of resistor R, -10 Vdc is applied across the input of the voltage divider R10, and then the voltage divider is trimmed to produce the desired "on" bias at the modulator audio input.

When the VOX is in the "off" condition, its output equals +2 Vdc and the negative bias at the modulator is equal to or greater than 4.3 Vdc. This is sufficient to reduce the modulator output to a negligible value.

The modulator load consists of a 22 megohm discrete resistor connected from gate to source electrodes of the MOS FET transistor used in the modulator. The resistor, in addition to forming part of the summing network, also serves to protect the transistor from voltage breakdown of the gate insulation due to static charges.

For duplex transmitters, the voltage divider, R10, is trimmed to the desired "on" bias without a VOX circuit or discrete resistor connected.

4.2.4 Voice Operated Switch

The purpose of the Voice Operated Switch (VOX) is to turn the simplex transmitter off, except when the operator is speaking (see Figures 21 and 22). The circuit is a conventional Schmitt trigger with a diode detection circuit at the input. The input signal is supplied by the audio amplifier and the output is fed through a discrete summing resistor to the gate of the modulator transistor. The output equals +8 Vdc when the input increases to 1.2 to 1.5 volts P-P (0.43 to 0.50 volts rms) and the output drops to +2 Vdc when the input decreases to 1 volt P-P or less (0 to 0.35 volts rms). In other

words, the transmitter is turned on for voice signals greater than 0.50 millivolts rms and is turned off for voice signals less than 0.35 millivolts rms. The switch turns on approximately 0.1 millisecond after its input voltage reaches 0.5V rms and turns off approximately 2 seconds after its input voltage drops below 0.35V rms.

4.3 Dual Receiver

The dual receiver consists of two identical VHF/AM receivers mounted on a common printed circuit board. One receiver termed "duplex" operates only when the duplex transmitter is operating, and the other receiver termed "simplex" operates only when the simplex transmitter is operating. The reason for specifying two receivers for the system was probably to achieve greater reliability through redundancy.

The desired performance characteristics are as follows: Input carrier frequency is 259.7 mHz ± .005%. Receiver RF input impedance should be nominally 50 ohms (antenna impedance) and receiver AF output impedance should be 600 ohms when measured at 1 KHz, single ended (headset impedance).

Receiver sensitivity should be sufficient to produce a signal plus noise-to-noise ratio of 10 db with an RF input signal level of 7 microvolts, modulated 30% with a 1 KHz reference tone. The audio output power should be continuously variable from 0 to 15 milliwatts.

The audio output frequency response should be flat within ± 3 db over the frequency range from 300 to 3000 Hz with a high

frequency attenuation of 6 db/octave beyond 3 KHz. The average noise figure of the receiver, measured between the receiver input and audio output, should be no more than 8 db.

The total distortion of the audio output with the maximum output power should not exceed 10%. An automatic gain control is provided in an effort to limit the audio output to a maximum increase of 10 db as the input signal level increases from 2 to 400,000 microvolts.

The local oscillator frequency should vary no more than ± .005% from the nominal frequency with the maximum extremes of voltage and temperature. The overall nominal I.F. bandwidth should be no less than 70 KHz at the 3 db points. Local oscillator frequency was selected to be 259.35 mHz; therefore, the nominal I.F. frequency is the input carrier frequency minus the local oscillator frequency or 350 KHz. With the ± .005% frequency tolerances, the IF frequency may equal 350 ± 26 KHz; therefore, the 70 KHz bandwidth is adequate.

Each receiver consists of a shielded RF section and an unshielded IF and AF section. See Sketch 9 and Figure 7. The RF section, housed in a grounded brass container, consists of a local oscillator, an antenna signal amplifier, and a mixer. The 259.35 mHz local oscillator consists of an 86.45 mHz oscillator, a tripler, and a tripler signal amplifier. See Sketch 9a and Figures 27, 28, 31, and 32.

The IF/AF section consists of two 1 inch x 3 inch substrates called "IF amplifier No. 1" and "IF amplifier No. 2." See Figures 23 through 26.

4.3.1 IF Amplifier No. 2

IF Amplifier No. 2 amplifies the 350 KHz intermediate frequency signal from the mixer, detects the audio signal from the amplified IF signal, and amplifies the audio signal. The nominal voltage gain is 100 db or 100,000. The IF amplification is performed with five amplifiers and six source followers; the AF amplification is performed with one amplifier and one source follower. A source follower is connected between the mixer and the first IF amplifier stage, between each IF amplifier, between the last IF amplifier and the detectors and between the audio amplifier and the headset. The source followers are used to prevent capacitive loading from one stage to the next.

A second detector converts the amplified IF signal to a negative dc bias voltage which is fed back to the gates of the first three IF stages for automatic gain control.

The fourth IF stage contains a feedback loop with a twin T filter. The filter is tuned to the nominal IF frequency of 350 KHz. The effect of the feedback is to convert the wideband amplifier to a narrow band amplifier with maximum gain at 350 KHz. This characteristic was included in the design to provide some degree of selectivity and noise reduction.

During debugging it was found necessary to add a 10,000 pf discrete "chip" capacitor between the audio detector and the audio amplifier in order to maintain the stage at zero bias. Without this capacitor, a positive bias builds up which causes saturation of the transistor. A 3900 pf capacitor would probably be large enough, since

that is the value of the coupling capacitor used between the audio amplifier and the final source follower. (The chip capacitor, which is about .020 inch thick, is mounted on the substrate over resistors R2Y and R3Y using epoxy cement.

The dc load for the fourth IF stage consists of a transistor in parallel with a resistor. The advantage of using a parallel resistor-transistor load is that the load can have a high value and the operating point can be located at a relatively high value of drain current, where transconductance is high, without the need for a high drain supply voltage. The high load resistance and high transconductance result in high voltage gain. Location of the operating point at a fairly high drain current also permits a large output voltage without saturation. If a parallel resistor is omitted, as was done in the audio amplifier, the above advantages are more pronounced, but the load transistor must be very closely matched to the amplifying transistor.

4.3.2 IF Amplifier No. 1

IF Amplifier No. 1 amplifies the 350 KHz IF signal from the mixer and rectifies the amplifier IF signal to provide dc signals for automatic gain control of the RF portion of the receiver. The nominal voltage gain is 900.

One rectifier (detector) provides zero bias plus a negative AGC signal which is fed back to the gate of the transistor in the antenna amplifier.

A second rectifier (detector) provides a negative bias plus a positive AGC signal which is fed back to the gate of the transistor in

the mixer. The 0 to -10 Vdc bias is obtained from a voltage divider, R7 and R8, which may be adjusted by trimming R8. Mixers require bias of approximately -3 Vdc. The optimum voltage is determined when the RF portion of each receiver has been assembled. (See note 7 for the RF schematics.)

The amplification is performed by four IF amplifiers and three source followers. A source follower is connected between each amplifier to prevent capacitive coupling from one stage to the next. The use of ac rather than dc amplifiers (direct coupled amplifiers) minimizes the effect of variation in the relationship between drain current and bias (instability) in the transistors and is therefore more compatible with the use of thin film, field effect transistors.

4.3.3 IF Amplifier Assembly

The assembly procedure is the same for both IF amplifiers, except as noted.

1. Select transistors for the IF amplifier stages which have relatively low transconductance (1000 to 3000 μmhos) and relatively high zero bias drain current (approximately 5 ma). This was found necessary in order to prevent instability (self-induced oscillation). If the gain is too high, instability, probably due to feedback through the B+ conductor, will result. The high drain current devices permit the use of a lower load resistance for lower voltage gain, without saturation of the output.

2. Connect the terminal pins and discrete components. Place the transistors with the lowest transconductance and highest zero bias drain current in the IF stages near the output end.

3. Increase the load resisters R2 in the last three stages sufficiently to prevent saturation, starting with the final amplifier. Maximum output of the audio amplifier is 15 milliwatts into a 600 ohm load. The maximum voltage output must therefore equal 3 volts rms or 8.5 volts P-P. The load resistor is generally trimmed to produce a drain voltage of +6 Vdc for amplifiers or a source voltage of +6 Vdc for source followers to obtain a maximum, unsaturated output voltage.

The load resistors in the initial stages are generally left at their minimum, untrimmed values, since their output voltages are low enough that saturation is no problem. If gain must be increased, however, the load resistors in the inital stages are increased, starting with the first stage.

4. For IF Amplifier No. 2, measure the capacitors in the tuned IF filter, calculate the resistance values required for minimum impedance at 350 KHz using one set of equations listed for the "Double Twin T Filter," and trim the resistors accordingly.

5. For IF Amplifier No. 1, trim R8 to produce the desired negative bias for the mixer.

6. It is generally not necessary to trim any other resistors, although trimmable resistors are available in all the detectors, except that for the mixer, such that detector characteristics may be varied somewhat.

4.4 RF Sections - Transmitters and Receivers

Because of their similarities, the RF sections of the transmitters and receivers are discussed together. Schematic diagrams

and photographs of the sections are shown in Figures 29 through 32. Figures 27 and 28 show the schematic diagram and substrate for the Universal RF amplifier. Sketches 8 and 9 are assembly drawings of the dual transmitter and dual receiver. The above documents, including the "Notes for the RF Schematics," provide sufficient information to assemble and trim the RF sections.

All stages are essentially narrow band amplifiers tuned to the desired radio frequency. Impedance matching between stages and from the last transmitter stage to the antenna load (via the diplexer) is accomplished by means of a variable inductance from drain (or collector) to ground of the source stage and a variable coupling capacitor between the drain (or collector) of the source stage and the gate (or base) of the transistor in the load stage or to the antenna load for the final transmitter stage. This circuit arrangement is used when the load resistance is less than the source resistance. The variable inductance is actually a parallel LC tank circuit with a fixed discrete coil and a variable discrete capacitor. The capacitor is tuned so that the tank behaves as an inductor at the operating frequency. The inductance is equal to that value required to neutralize the output capacitance of the source stage and the input capacitance of the load stage plus whatever additional inductance is required for impedance matching between the source and load resistances. The coupling capacitor must also have a certain value for optimum impedance matching. Impedance matching results in maximum power transfer, and, because the reactive components of

source and load are neutralized, this results in maximum voltage gain.

At one location, the load resistance is greater than the source resistance. This occurs at the input to the antenna amplifier of the receiver. Impedance matching is accomplished here by means of a capacitance from the input terminal of the load resistance and ground and an inductance between the output of the source and the input terminal of the load. The input capacitance of the transistor load is slightly higher than the optimum capacitance; therefore, a parallel inductance or inductive tank would be necessary to lower the effective capacitance to the correct value. Addition of a tank is not considered worthwhile since it would only increase the voltage ratio by 16%, assuming an infinite Q. Since the Q of tanks in series with the bypass capacitors are low, as will be seen later, a tank was omitted at the antenna amplifier input. A variable inductance between the antenna and antenna amplifier is achieved by means of a fixed coil in series with a variable capacitor.

In coupling between the antenna amplifier and mixer and between the local oscillator (tripler amplifier) and the mixer, an impedance matching network was omitted since the mixer input resistance is close enough in value to the output resistances of the above amplifiers that a matching network would be of little value. In this case, thin film bypass capacitors are used for coupling, and the tanks are used only for neutralizing transistor capacitances.

A fixed, thin film capacitor could probably have been used to couple the antenna load to the last transmitter stage since the

output resistance of the 2N3553 transistor in this stage is only about 75% higher than the 50 ohm load. Use of a variable coupling capacitor located in the diplexer simplified the construction at no cost in space, however.

At all other locations, variable coupling capacitors were considered to be worthwhile. Although they were not used between the oscillators and triplers, debugging indicates they probably would have been useful at these locations also.

In the use of parallel LC tank circuits, it is very important that the Q of the circuit have a high value. The equivalent circuit of an LC tank includes a parallel resistance which decreases as the Q decreases. If this resistance is low enough, it will load down the preceding stage and result in low voltage gain.

As an example of how Q effects the gain, consider tripler amplifier No. 2 for the transmitter where the transistor characteristics are nominal and no saturation occurs. For infinite Q capacitors and inductors and zero resistance conductors, the calculated voltage gain is 10.5. For an amplifier assembled with discrete components, including large, variable capacitors, and with a 50 millivolt P-P input, the measured gain is 9.2 v/v. When small variable capacitors are substituted, the calculated gain drops to 7.6 v/v. When a thin film circuit is used with the small variable capacitors, the calculated gain drops to 4.9 v/v. The additional drop calculated for the thin films is due primarily to about 1.6 ohms resistance in the thin film conductor from the tank bypass capacitor

to ground. This can be reduced to about 1 ohm by jumpering part of the conductor with a 5 mil dia. gold lead. (These resistances include skin effect at 300 mHz.)

The large variable capacitors, which were used in the breadboard models, were "ERIE NPO 2-8" capacitors with an equivalent series resistance of 0.26 ohms and the small variable capacitors were "JFD-MT-209" or "JFD-MT-220" which have an equivalent series resistance of 0.67 ohms. Since capacitor Q at high frequency is the ratio of reactance over resistance, it is seen that, at a given capacitance and frequency, the Q of the large capacitor is 2.58 x that of the small capacitor and 6.15 x that of the thin film capacitor without the wire jumper. The wire jumper improves the Q of the thin film capacitor, C4a, by about 60%.

For a typical coil of .031μh (1.5 turns, 0.2 inch inside diameter, .025 inch wire diameter), the equivalent series resistance is 0.25 ohms at 300 mHz with .010 inch thick grounded brass plates located .020 inch from each end. The coil Q is reduced considerably if it is located too lcose to the brass container or if it is mounted on top of the variable capacitor or over any thin films. In the case of oscillators, it was found that oscillation will not occur if the coil is located over the films.

The main problem encountered with the RF sections was low gain in the tripler amplifiers and in the antenna amplifier. This was a particularly severe problem in the transmitter because the maximum unmodulated output obtained, without biasing the modulator,

was 10.8 volts P-P, instead of the needed 15.5 volts P-P. When the modulator was biased to cut this output in half for modulation purposes, the unmodulated power output was only 73 mw, compared to the 150 mw sought. In the receiver, the RF gain was not as critical because of the high IF gain, although a higher RF gain might have improved the signal to noise ratio.

In the transmitter RF section, the main problem was insufficient RF voltage into the modulator. For desired output, 8 volts P-P were needed, but actually only 2 to 3 volts P-P were realized. The tripler output was typically about 1 volt P-P; therefore, a gain of 8 was required. After accounting for the low Q of the thin film circuit with small variable capacitors, which resulted in the calculated gain dropping from 10.5 to 4.9, a decision was made to add a second tripler amplifier stage. Unexpectedly, however, the second stage had negligible effect in improving the overall gain. There was no evidence of clipping or distortion in the signals that would result from saturation, but this effect may have been masked by the filtering action of the tank circuits.

It was found, both theoretically and experimentally, that the second power stage (class C) of the original design could be eliminated. The reason for this is that the output resistance of the 2N3553 transistor in the first power amplifier and the input resistance of the 2N3553 transistor in the following stage are so low that the first power stage, instead of amplifying the signal, had an attenuation of about 0.8 volts/volt.

Elimination of this stage would also have the advantages of providing room for the second tripler amplifier, save power, and lead to greater linearity because there would be fewer stages between the modulator and the antenna, and because all stages are now operated class A.

The second major problem with the RF sections was the difficulty of making reliable, low resistance joints. The wire leads had to be reasonably large in diameter (.018 to .025 inch) in order to minimize the resistance at high frequency due to skin effect so that the circuit Q would be reasonably high. In an effort to improve the joints, the thin film terminals were changed from the conventional aluminum over chromium to copper over chromium and the wires were then fastened to the films with lead-tin solder, using a small soldering iron. This improved the joints considerably, but some of the terminals were no larger than the wires being soldered to them and the stresses resulting from normal handling during assembly and checkout, frequently resulted in failure of the joints.

In actual assembly, it was found that the geometrical layout of the Universal RF amplifier made the assembly of discrete components very difficult. This also might lead to possible unreliability, even when extreme care is exercised in handling the circuits.

4.5 Dual Diplexer

The dual diplexer consists of two identical transmit-receive diplexers mounted side by side on a common printed circuit board (see Sketch 6 and Figure 2). One diplexer is used during the simplex mode

and the other is used during the duplex mode of operation. The function of each diplexer is to channel the incoming 259.7 mHz signal from the antenna to the receiver and to channel the outgoing 296.8 mHz signal from the transmitter to the antenna, for simultaneous transmission and reception.

Each diplexer is required to exhibit 60 db attenuation from the transmitter to receiver terminal and must not have more than 1 db insertion loss from the terminal to the antenna. The in and out impedance of each diplexer must match the impedance of the receiver and transmitter connected to it and must match an antenna of 50 ohms, nominal.

The final diplexers met all the objectives, except the insertion loss was 3 db instead of the maximum desired 1 db. Thus, 50% of the signal power is lost in traveling through the diplexer, instead of the maximum anticipated loss of 20%.

The prototype model of the diplexer had an insertion loss of 1 db. The only difference in the final design model and the prototype model was the type of variable capacitors used. The prototype model contained ERIE NPO series capacitors with an equivalent series resistance of 0.26 ohms at 250 mHz, and the design model contained JFD-MT 200 series capacitors with an equivalent series resistance of 0.67 ohms at 250 mHz. Thus, the Q of the prototype model capacitors was higher than the Q of the design model capacitors by a factor of 2.58. The lower capacitor Q is believed to be responsible for the higher insertion loss in the design model of the diplexer.

The reason for using the JFD capacitors in the design model was because of their smaller size. Had the large ERIE capacitors been used, the diplexer would be 0.18 inches thicker, with a volume increase of 2.63 cu. in.

4.6 Coaxial Switch

The function of the coaxial switch is to connect the antenna to the duplex diplexer during the duplex mode of operation and to connect the antenna to the simplex diplexer during simplex operation such that the antenna is connected to either the simplex or duplex system, but not to both simultaneously.

The coaxial switch is a latching relay which is switched by application of battery voltage via the rotary selector switch for a maximum of 10 milliseconds. Once switching is completed, the dc input to the coil is automatically disconnected. The switch is manufactured by Electronics Specialty Co., Los Angeles 39, California, part no. 13-12-03240.

The switch has an insertion loss no greater than 0.5 db (10.87% max. power loss) and a voltage standing wave ratio (VSWR) no greater than 1.5 to 1.

4.7 DC Power Supply

The dc power supply converts the 37.4 to 27.5 Vdc supplied by the battery to the following regulated dc voltages: +3, +10, +12, +25, and -10. A wiring diagram of the supply is shown in Figure 8, and an assembly drawing of the supply is shown in Sketch 7. Each output voltage is regulated to an accuracy of ± .05%, except for the

+25 Vdc output which is regulated to an accuracy of ± 0.32%. The maximum power required for +3, +10, +12, +25, and -10 Vdc outputs are .03, 0.54, 0.60, 2.50, and .02 watts, respectively. The peak input power required is 7.27 watts. Thus, the overall efficiency at peak load is 50.7%.

4.8 Final Test and Debugging

During this phase, copies of the individual modules designed and first built under Phase B were made in sufficient quantity to produce two complete prototype TFPCTS units. After these modules were made, they were integrated into the overall system design. Problems discovered in debugging the modules and the system itself have been discussed in detail in the individual preceding sections and in supplied failure reports. All problems associated with normal debugging were corrected, and the unit was assembled into the final package. When tested in accordance with the test procedure in Appendix B, the total units were not measurably operable. Changes beyond those already accomplished in the debugging would require research and development effort and a major redesign which are beyond the scope of the contract.

4.9 Test Results Analysis

A detailed study of the causes of the inoperability of the final units has not been made. However, a number of factors which were uncovered in the debugging of the assembled modules indicate what the source of major unexpected problems may be or at least indicate a direction and approach for further investigation.

When the contract was awarded, there was serious doubt that an active thin film device could be developed in time for use in this program. Likewise the factors involved and the full impact of the use of mask deposited thin films and circuit operation at 300 MHz on circuit designs were not known or fully appreciated. The contract anticipates difficulty in developing the thin film device and designing the needed system modules since it provides for separately approved phases. As originally analyzed with thin film knowledge and experience available at the completion of Phase A, it appeared to be a fairly reasonable assumption that the breadboard from Phase A could be literally translated into thin film form. The unanticipated problems that were actually experienced in the integration phase, which were outside the scope of the contract, can be classified into the following basic areas:

a. Unexpected electrical interaction of components and thin films and their intensification at the 300 MHz frequency. An example of this is the degradation of coil performance when placed over any thin film.

b. Unanticipated extreme effect of changes in component values within tolerance on the operation of the system. Certain transistors had to be screened to select operating characteristics at a specific point in its tolerance range to match specific circuits.

c. Unanticipated and unexpected mixmatches and effect of tolerance accumulation between modules in the system after integration.

While the work performed on this program does not provide positive solutions to all of the problems experienced in integrating

the system into a working unit, it does provide information on the research and development efforts remaining. Our recommendations for this work are discussed in the next section.

5. RECOMMENDATIONS FOR FUTURE WORK

During the integration, debugging and final assembly of the TFPCTS certain trouble areas and potential sources of failure involving further research and major redesign were identified. While it was not within the scope of the present contract to perform this additional research and redesign of the modules and systems, these problem areas should be considered in a future program for this system. The investigation and major redesign is needed if a TFPCTS is to be developed to meet the objectives of NASA as modified in this contract, that is an operating thin film hybrid circuit system. If the original objective of an all thin film system including active devices is still desirable, additional research is needed.

The recommendations below are limited to those areas of future investigation of the hybrid thin film system as seem to be indicated by the results of work on this program.

5.1 Radio Frequency Sections

An investigation of the effect of replacing the 2N3823 junction FET's with insulated gate (MOS) FET's such as the K1202 seems desirable based on the results of debugging the prototype units. It seems possible that part of the problem of unexpected low gain, especially in tripler amplifiers, may have resulted from forward biasing of the junction of the N type junction, field effect transistor, during the positive half cycle of the input signal,

considering that the gates were at zero dc bias. If this occurs, then the junction conducts when positive with respect to the source and this might result in clipping or effective saturation and noise generation during the positive half of the cycle. It appears that this problem would be especially severe where large input signals are encountered, such as 1 volt p-p into tripler amplifier No. 1 and at least 3 volts P-P into tripler amplifier No. 2 of the transmitter and may explain why the combined gain of the two amplifiers was only about 3.8 v/v instead of the calculated 24 v/v. The needed output of the two stages is 8 volts P-P with a 1 volt P-P input. Even considering normal saturation due to operation along the AC load line within the pinch off region of the I-V curves of the transistor, one would expect an output of at least 8 volts P-P. (The calculated gain of 4.9 v/v per stage, includes the effect of the low Q tank circuit.)

Based on our experience with the assembly and tests of the prototype, redesigning the RF sections so that one substrate approximately 1" x 3" in size contains the entire RF section of the transmitter and another substrate of similar size contains the entire RF section of the receiver likewise seems warranted. This might be done in lieu of using up to eight 1" x 0.5" Universal RF substrates for each section, as is done in the present design. Aluminum could be used only for capacitor plates and copper over chromium layers might be used for all conductors and terminals. It

appears that dimension of the solder terminal should be at least twice as large as the diameter of the wire to be fastened for best results. All wire leads would be soft copper or gold and discrete components would be positioned and fastened to the substrate in a manner that facilitates soldering of leads and minimizes stress placed upon the solder joints by leads.

Our results indicate that all conductors forming portions of tank circuits should be as short and as wide as possible to minimize resistance and inductance. Where appreciable lead inductance is unavoidable, it should be estimated and taken into account in redesigning the thin film capacitors. These estimates would be utilized in test samples and verified before redesign finalization and fabrication.

The use of thin film inductors instead of discrete coils appears to deserve reconsideration. They were not used in the present design because of low Q's, but this problem might be overcome by tinning the Cr-Cu spiral inductors with solder to reduce the resistance to an acceptable level. Where high value tank inductances are required, a thin film capacitor might be deposited in parallel with a small inductor to increase the effective inductance. A variable capacitor in parallel to the thin film capacitor and inductor might still be needed for precise tuning, but it need not have large values.

A variable capacitor would be procured or designed such that its Q is increased to a level corresponding to an effective series resistance of 0.25 ohm or less at 300 MHz. It would feature a mounting flange or tabs that could be soldered to thin film pads, a stronger mechanical connection between the screwdriver drive and the rotor, and the smoothly moved rotor.

Experience indicates that trimming provisions for resistors and capacitors should be eliminated or at least minimized in any redesign. Unnecessary trim sections waste space and may have resulted in increased resistance and inductance in capacitor leads.

In redesigning resistors, the unexpected large decrease in resistance at high frequency encountered must be accounted for, especially for high value resistors. For example, resistor Ria decreased from 311 to 300Ω and resistor R2 decreased from 37K to 12K ohms as frequency increased from 0 to 250 MHz. Also resistor areas must be large enough to dissipate the heat they generate. Generally 100 watts/in^2 for resistors on Corning Code 0211 glass is considered safe, although the 250 ohm load resistors, Rla, of this design often dissipated up to 400 watts per square inch without failure.

In connection with this, it seems possible that the power stage of the transmitter may have experienced thermal run-away on several occasions because the 10 ohm load resistor burned out a few times. With normal collector current, it does not appear that this

should not have occurred. It may be advisable in a redesign to place a small resistor, about 1 ohm, in parallel with a bypass capacitor, from emitter to ground so that the transistor is biased off if the collecor current becomes too large.

On the basis of our experience in the integration phase, it now appears doubtful that RF shielding is needed between each stage. An investigation should be made to determine if and where the brass shielding partitions might be eliminated in order to simplify the design.

There is an indication that the use of single substrates for entire RF sections would greatly facilitate the assembly and might simplify the brass container and the printed circuit board. The number of interconnections and wire or printed conductors might also be reduced. Conductors would be shortened, unnecessary thin film components might be eliminated, and components could be arranged in an orderly and efficient manner so that discrete components might be more easily installed. The overall size of the receiver and transmitter might be reduced and be made to fit in the existing system package, even with the redesign changes.

5.2 Voltage Controlled Oscillators

A problem encountered with some of the VCO's of the telemetry unit was age stability of the resistors which resulted in frequency drift as high as 50 Hz over 2 to 7-day periods. This appears to have been caused by increases in resistance as high as 1%. The unexpected increase in resistance is believed to have

resulted from exposure of the rhenium film to air with subsequent oxidation possibly along the edge where the resistor film was cut away during trimming. The exposure is believed to have resulted from accidential chipping away of the SiO protective film during the cutting operation. Since some of the resistors had been narrowed from 5 to 2.5 mils wide in an effort to raise their values, a loss of SiO film 1% or .025 mil from the edge of the resistor could account for a 1% rise in resistance, assuming complete oxidation of the exposed Re. (Age stability tests of Re film resistors at temperatures up to 400°C in air indicate excellent stability, provided they are completely coated with an SiO film.)

Possible solutions to the problem are to make the resistors wider, use a thinner SiO film that is more stress free and less likely to chip or peel off the substrate when cut, and/or apply an oxygen protective coating immediately after trimming.

5.3 Tolerances

It now appears that the unusual step of specifying tolerances on characteristics may be needed for all components, circuit modules, sub-systems, and the overall system even with the system breadboarded. In general, mathematical equations could be written to define all functions in the light of our present experience. The accuracy of the equations should be checked experimentally and after their accuracy has been proven to be adequate, the equations might be used to calculate these tolerances.

In a thin film circuit, it is difficult, and generally impossible, to change component values after the deposition masks have been designed, unlike conventional circuits composed of discrete components. As a result, unlike conventional practive, it seems that design values cannot be estimated but must be accurately determined and verified. A breadboard model is useful for checking the accuracy of the system equations, but it appears that it cannot be relied upon to determine tolerances.

In addition, our tests show that the skin effect for a 0.12 ohm/sq. Al film results in an increase in resistance of 40% as frequency increases from 0 to 250 MHz. (Length of the conductor tested was 0.345 inches and width was .043 inch.)

In calculating capacitor Q, however, it seems we must assume the equivalent series resistance will increase by a factor of 2.5 from 0 to 250 MHz. This might take into account other factors effecting Q at high frequency, such as spread out of aluminum at the edges of the mask. The spread out portion is relatively thin and therefore has higher sheet resistance which increases the series resistance of the capacitor. The "spread out" effect increases as capacitor dimensions become smaller because the thin "spread out" portion represents an increasing percentage of the thick portion of the plates. "Spread out" increases as mask to substrate clearance increases and as film thickness increases. For the RF circuits, it was about 1 mil.

Based on the information developed from further study, each module could be reevaluated and any needed redesign could account for these new factors. After redesign, each module would have to be tested and the modifications verified before prototype modules could be fabricated and reintegrated into the system.

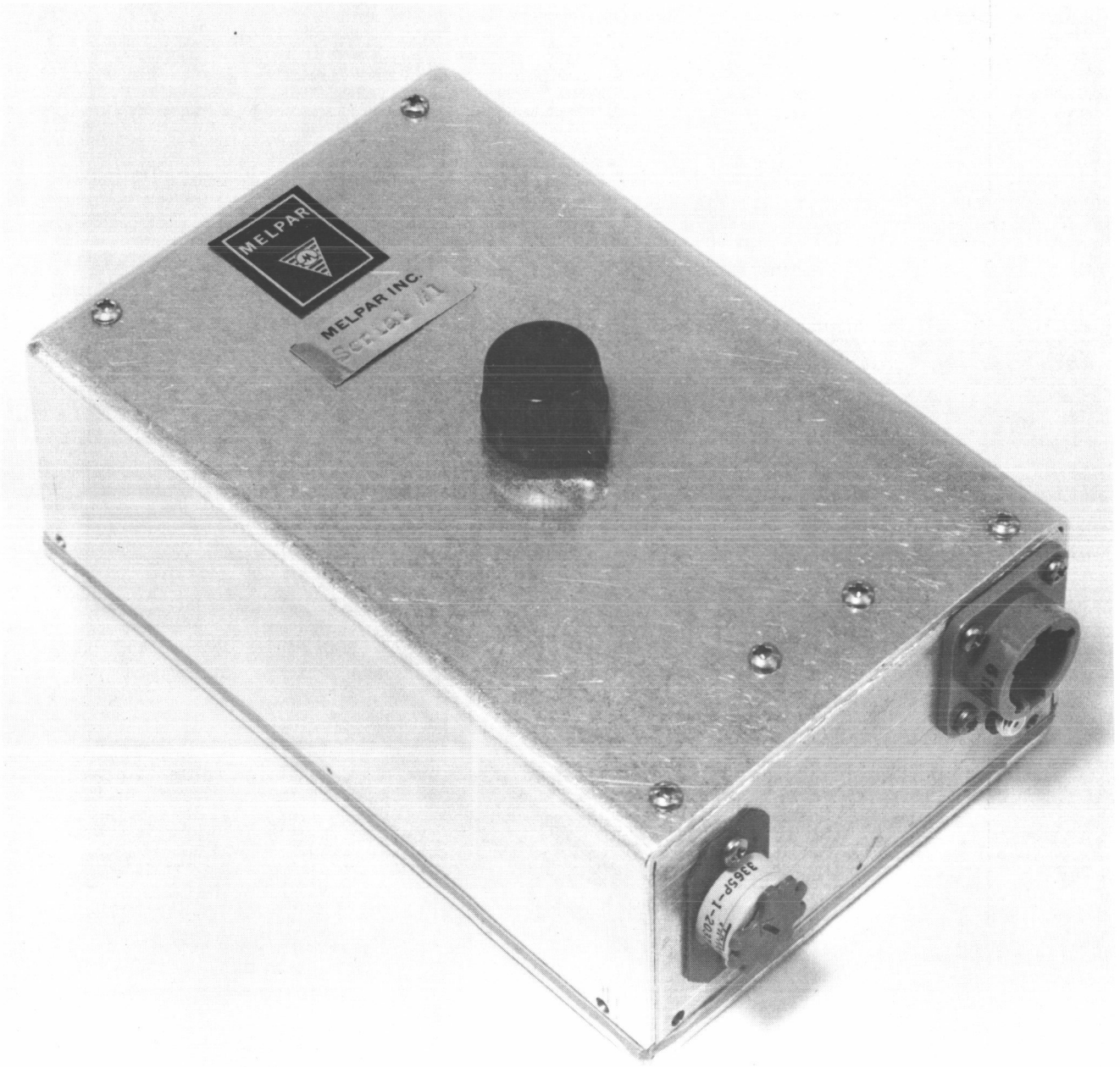

Figure 1. System Package

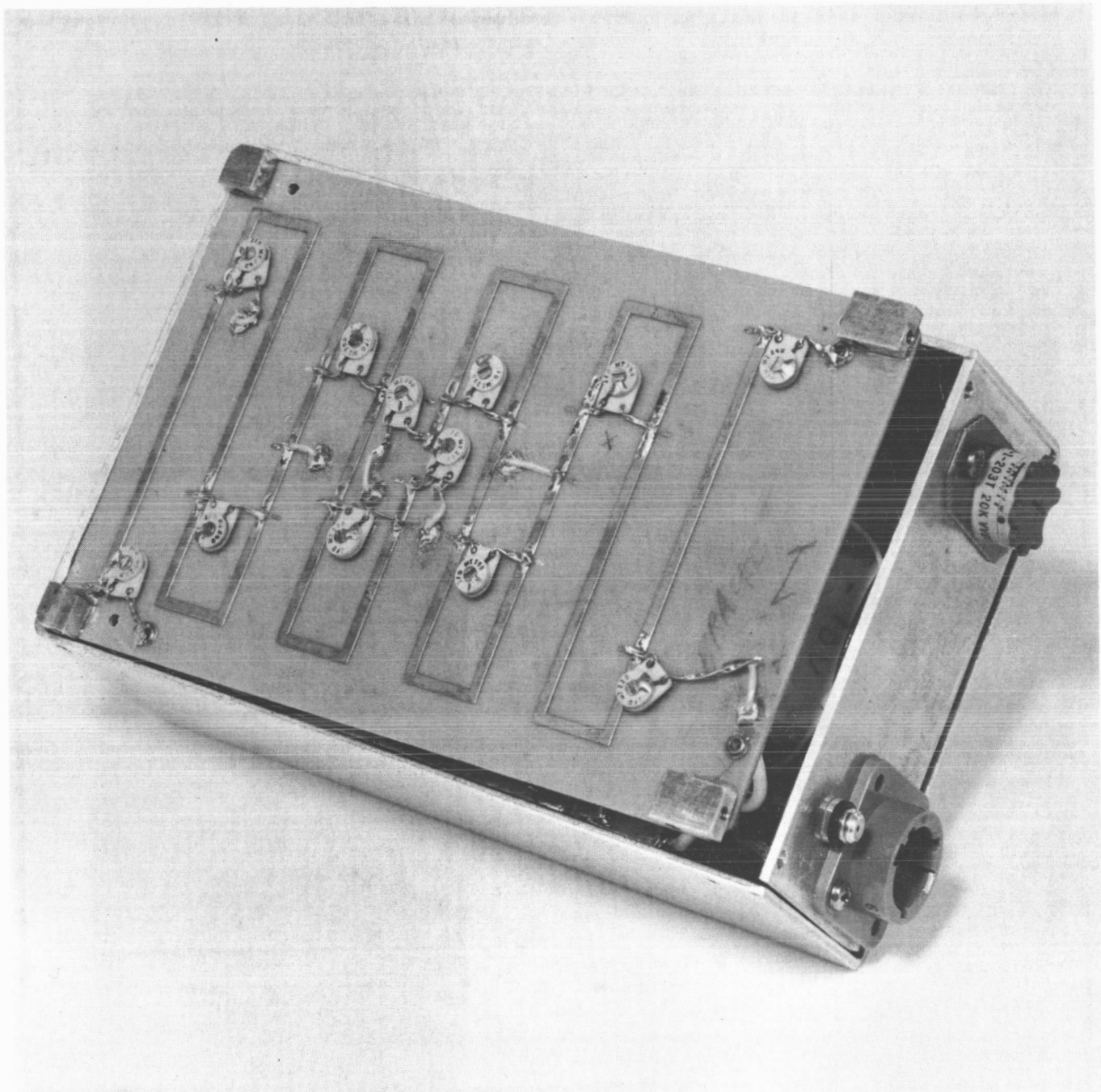

Figure 2. System Package with Cover Removed

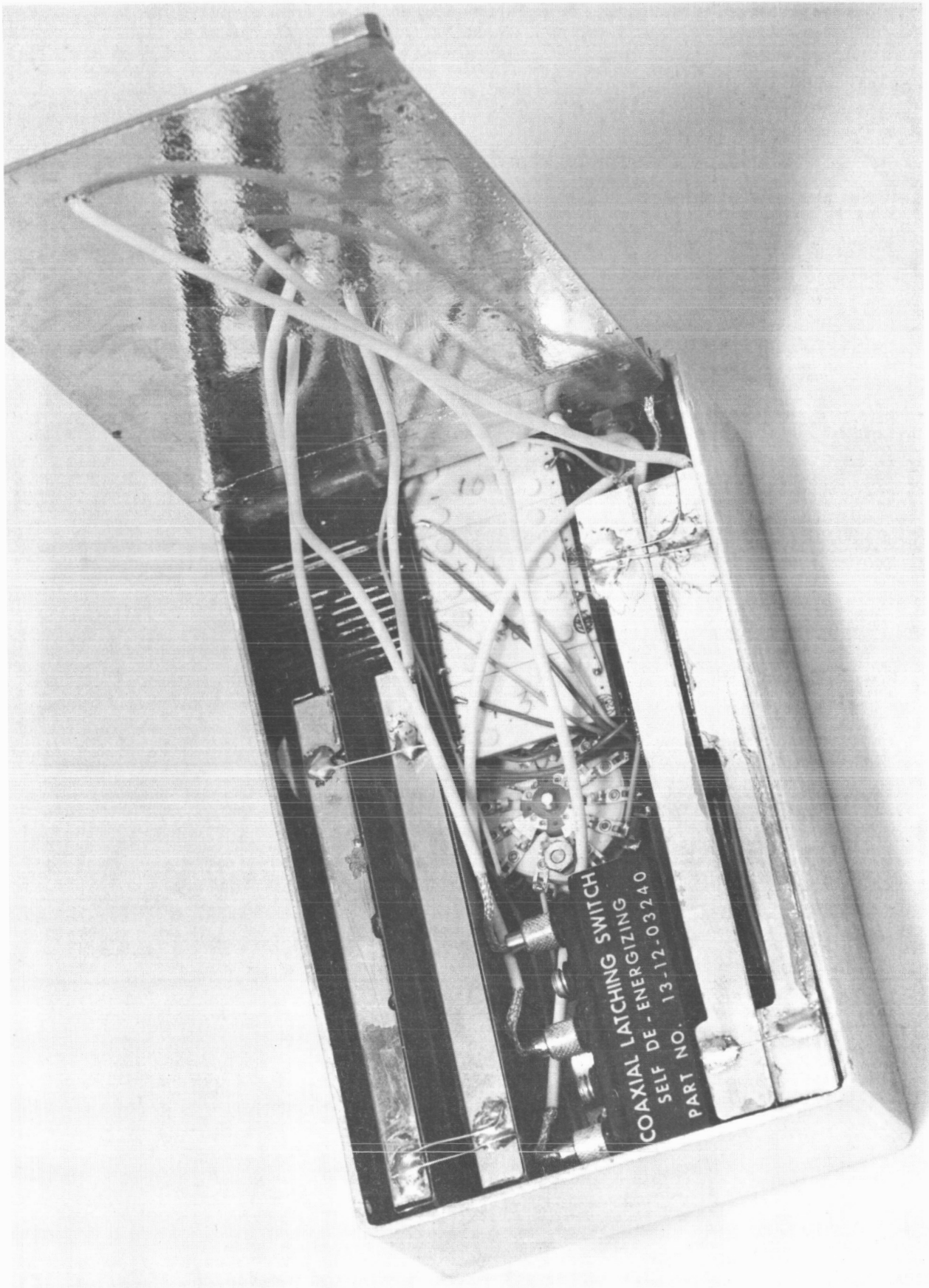

Figure 3. System Package with Cover Removed and Diplexer Swung Open

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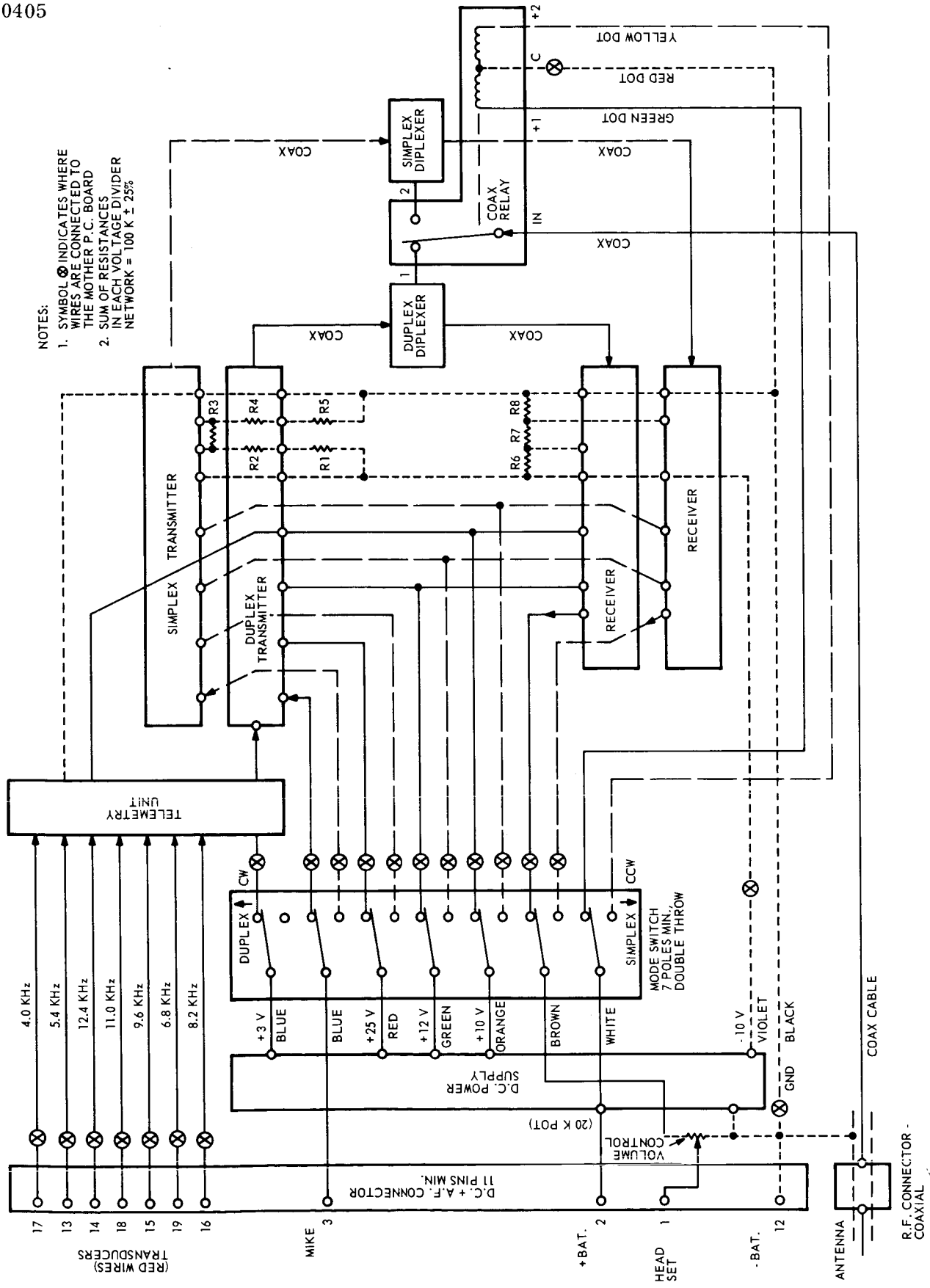


Figure 4. Wiring Diagram - Personal Communications and Telemetry System

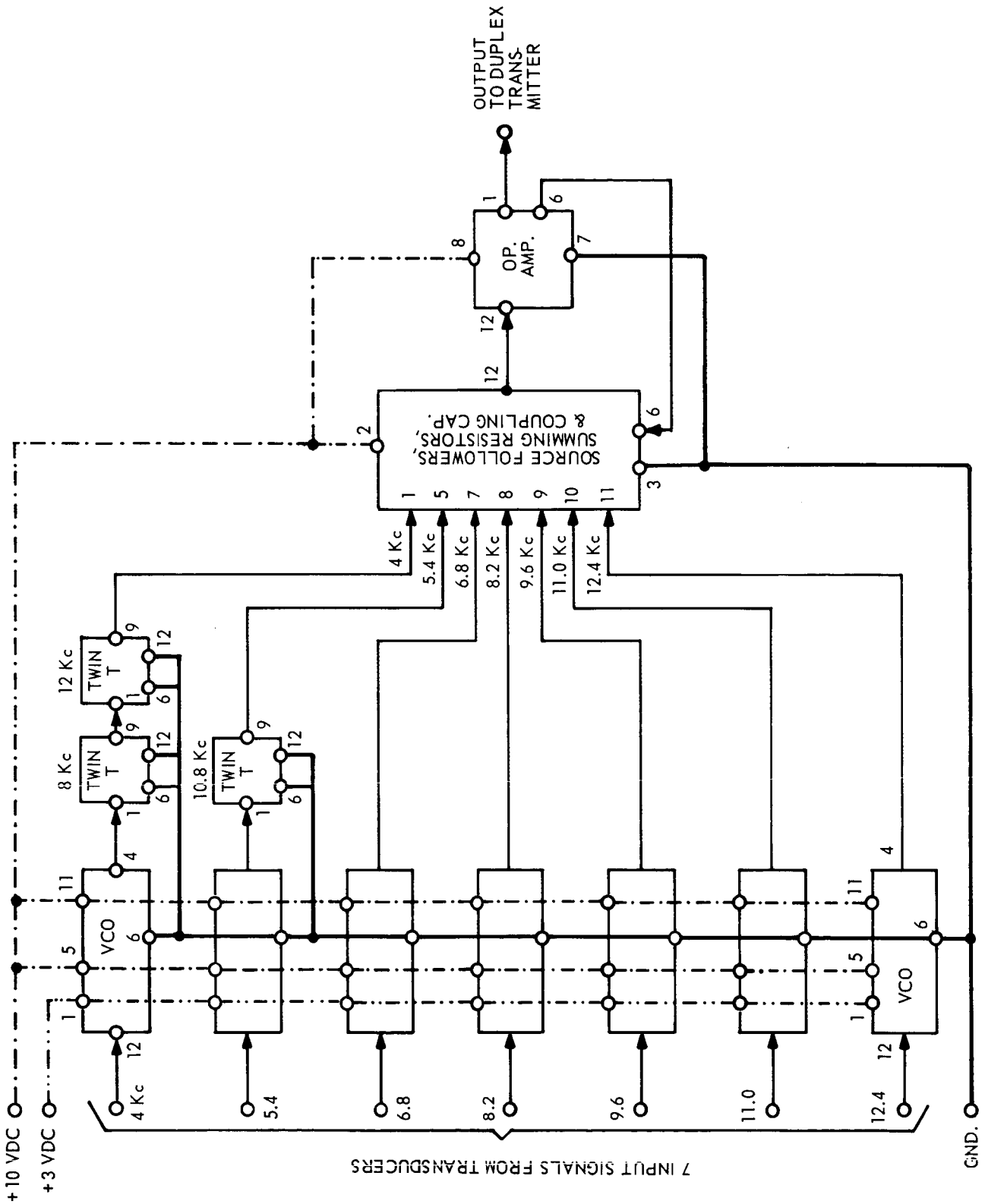


Figure 5. Wiring Diagram - Telemetry Unit

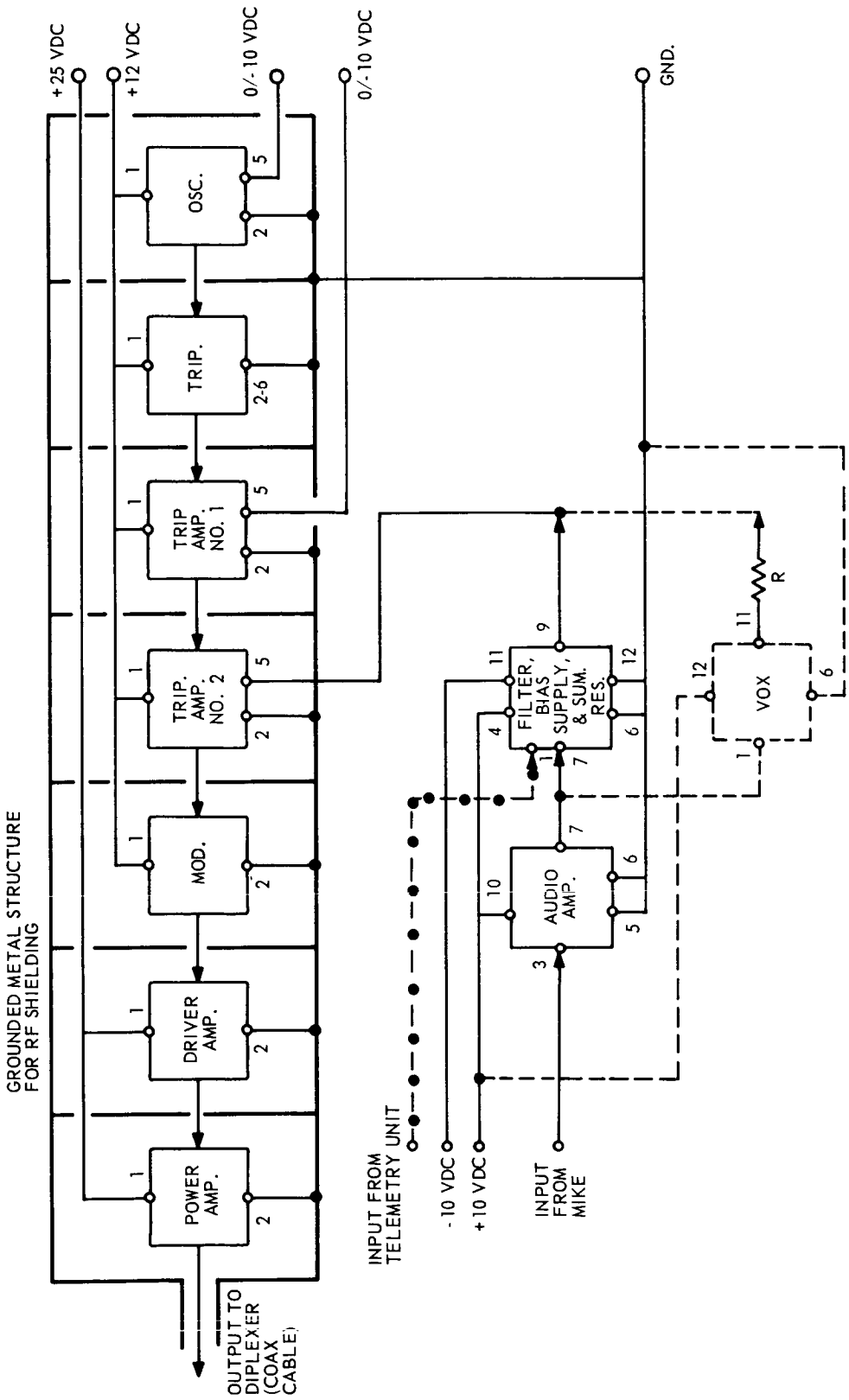


Figure 6. Wiring Diagram - Transmitter

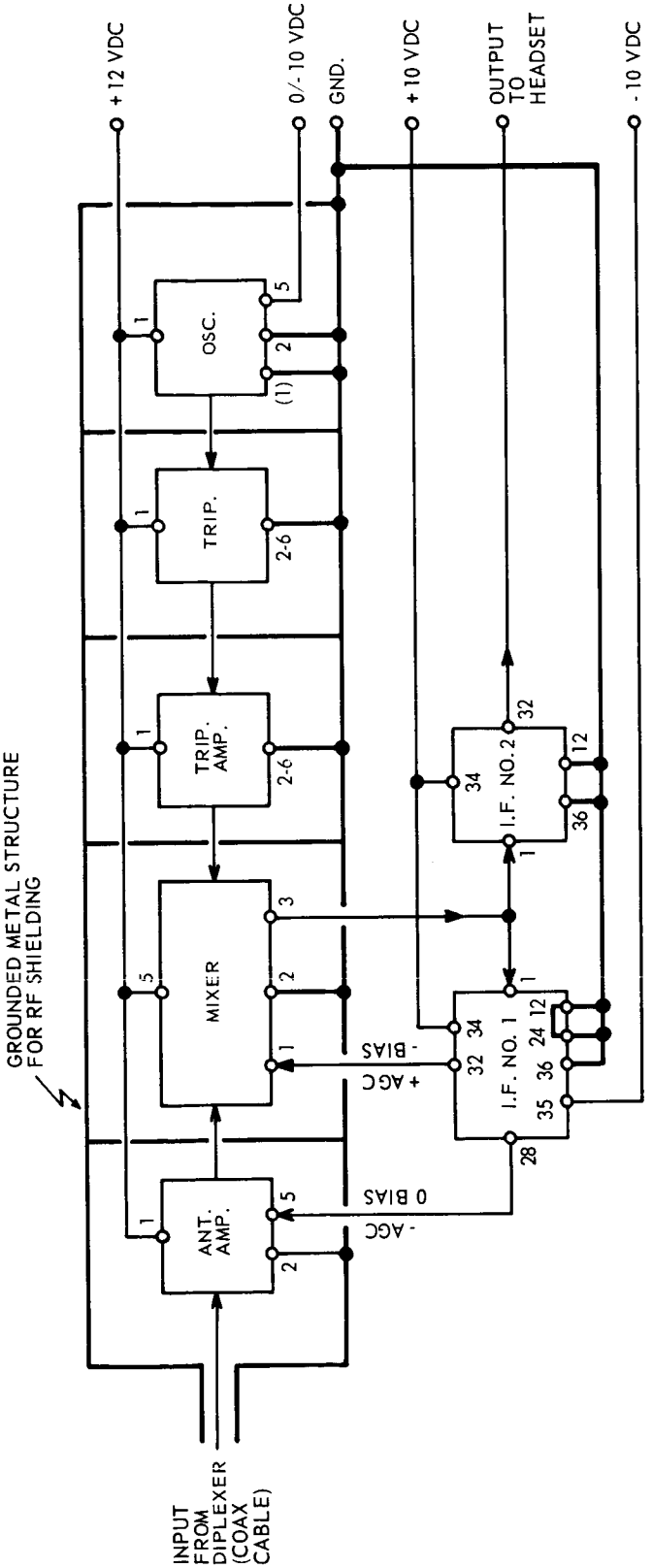


Figure 7. Wiring Diagram - Receiver

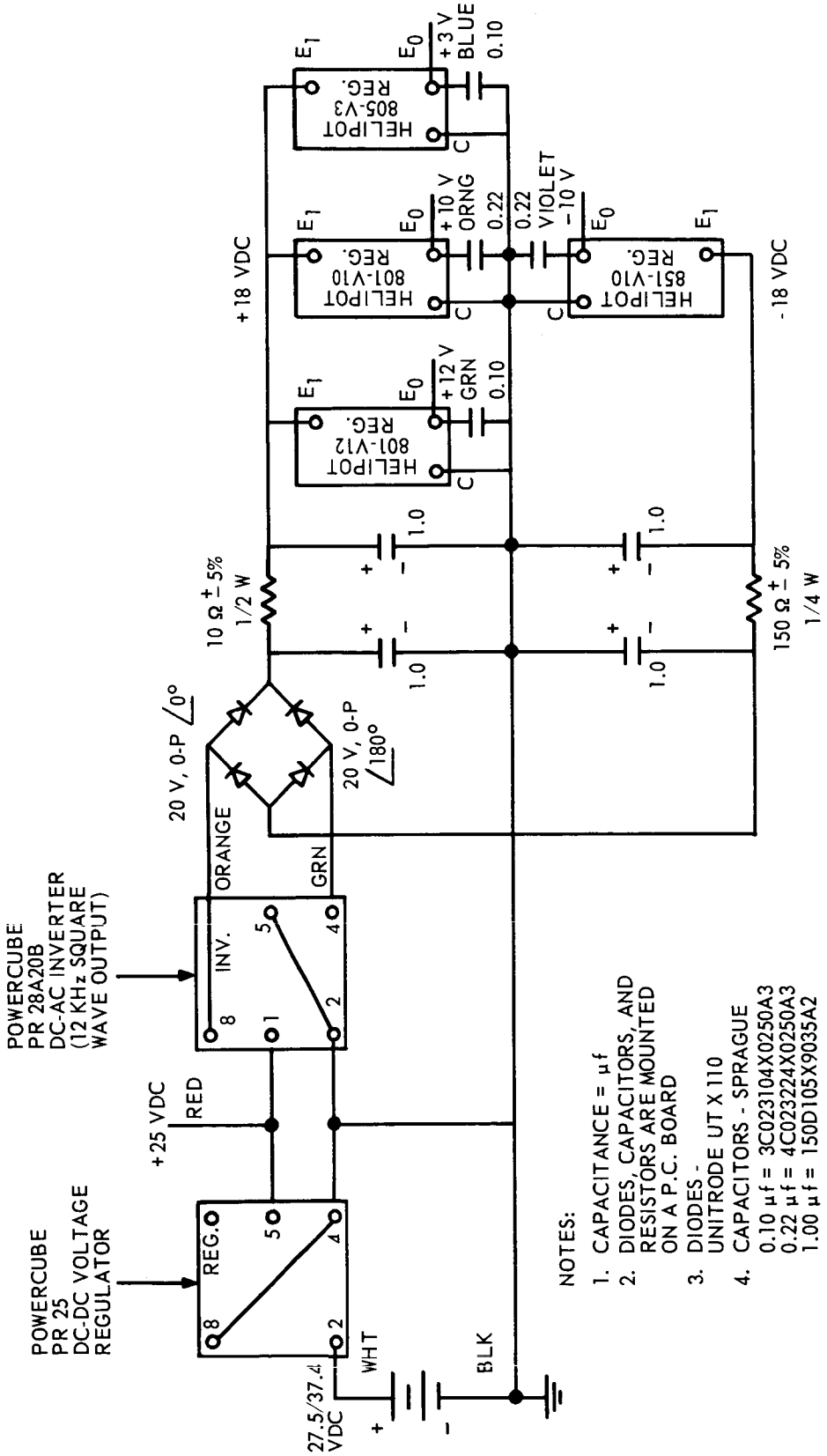


Figure 8. Wiring Diagram - dc Power Supply

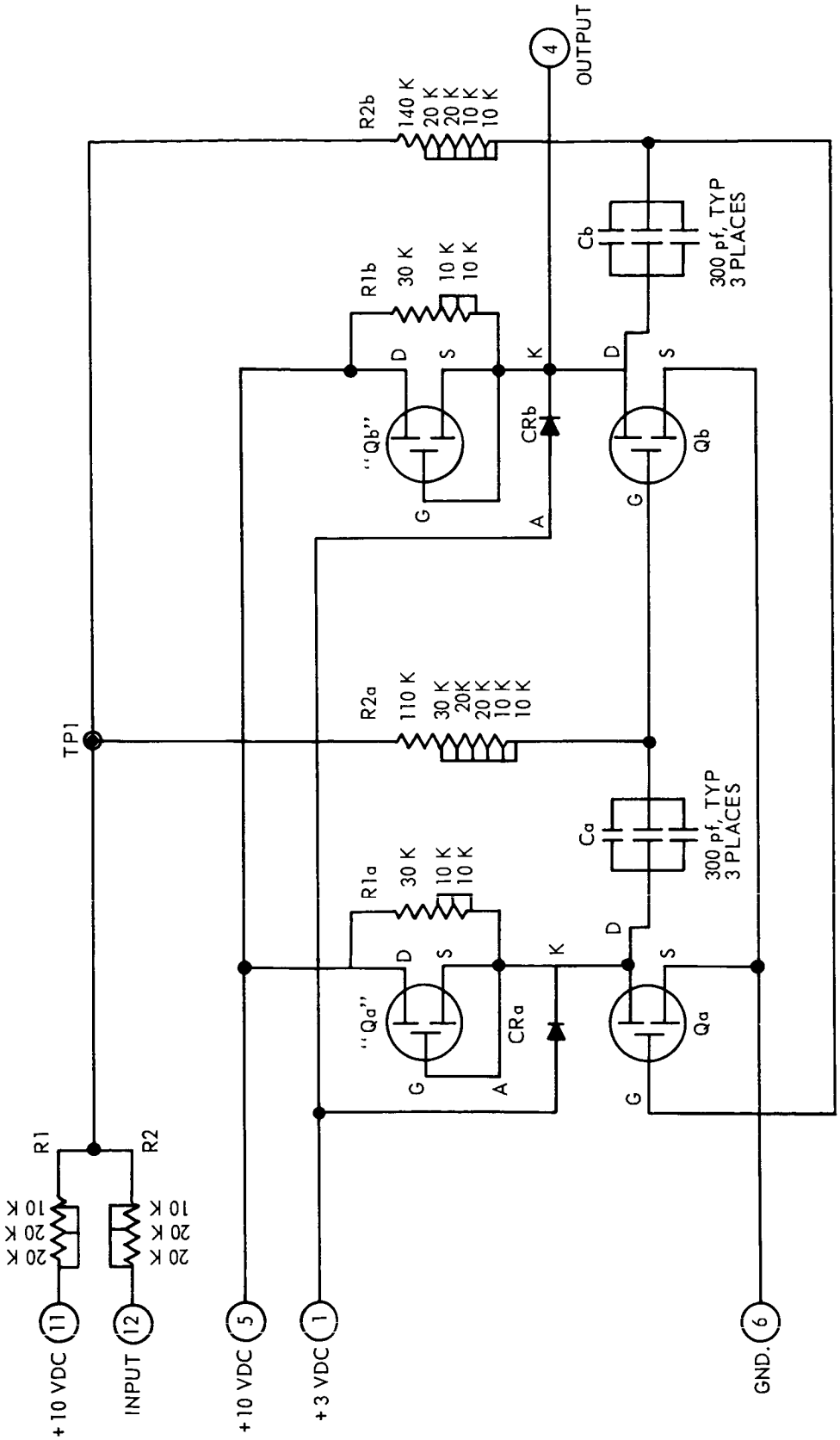


Figure 9. 5006-8 Voltage Controlled Oscillator - Schematic

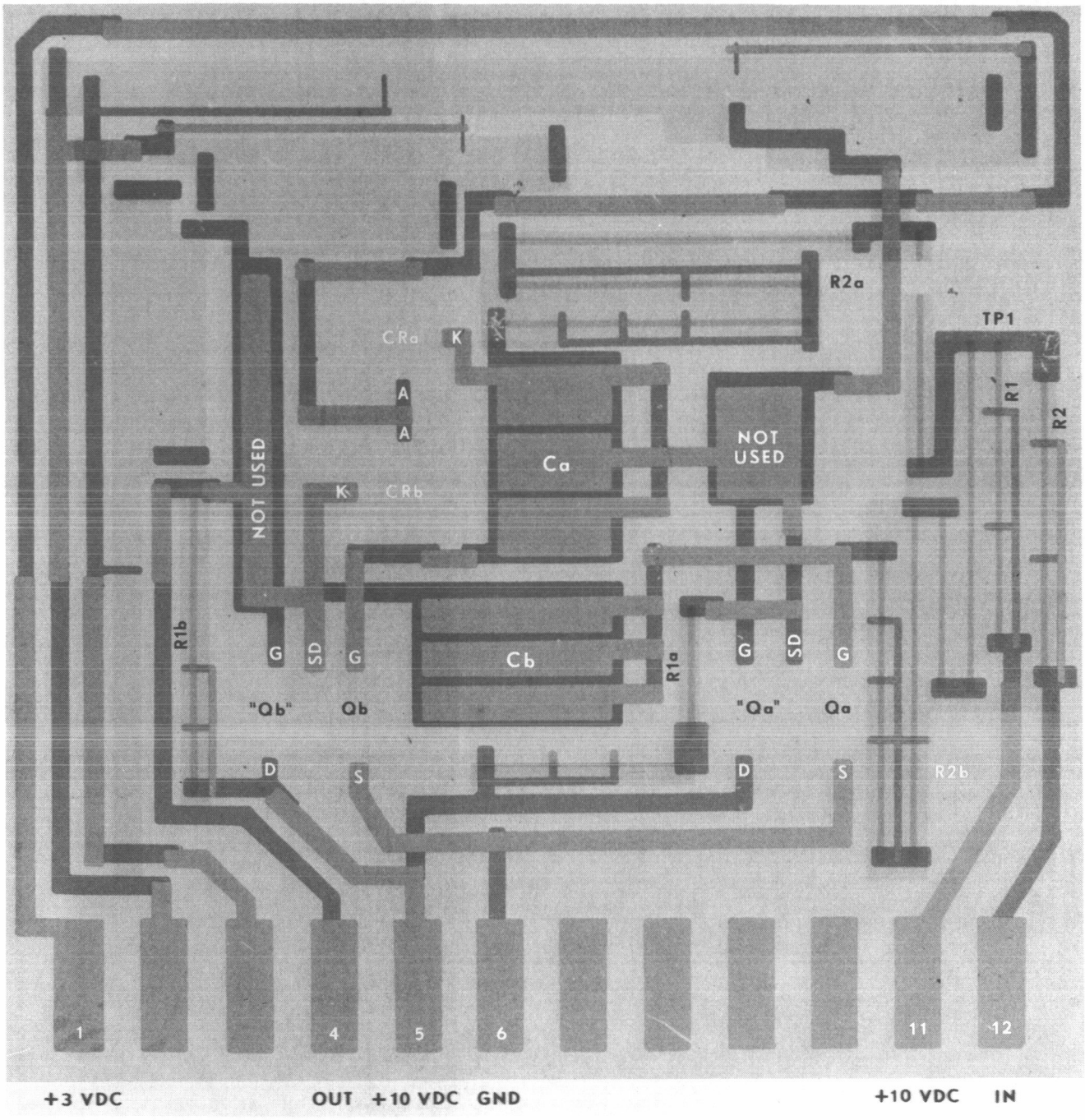


Figure 10. 5006-8 Voltage Controlled Oscillator - Substrate

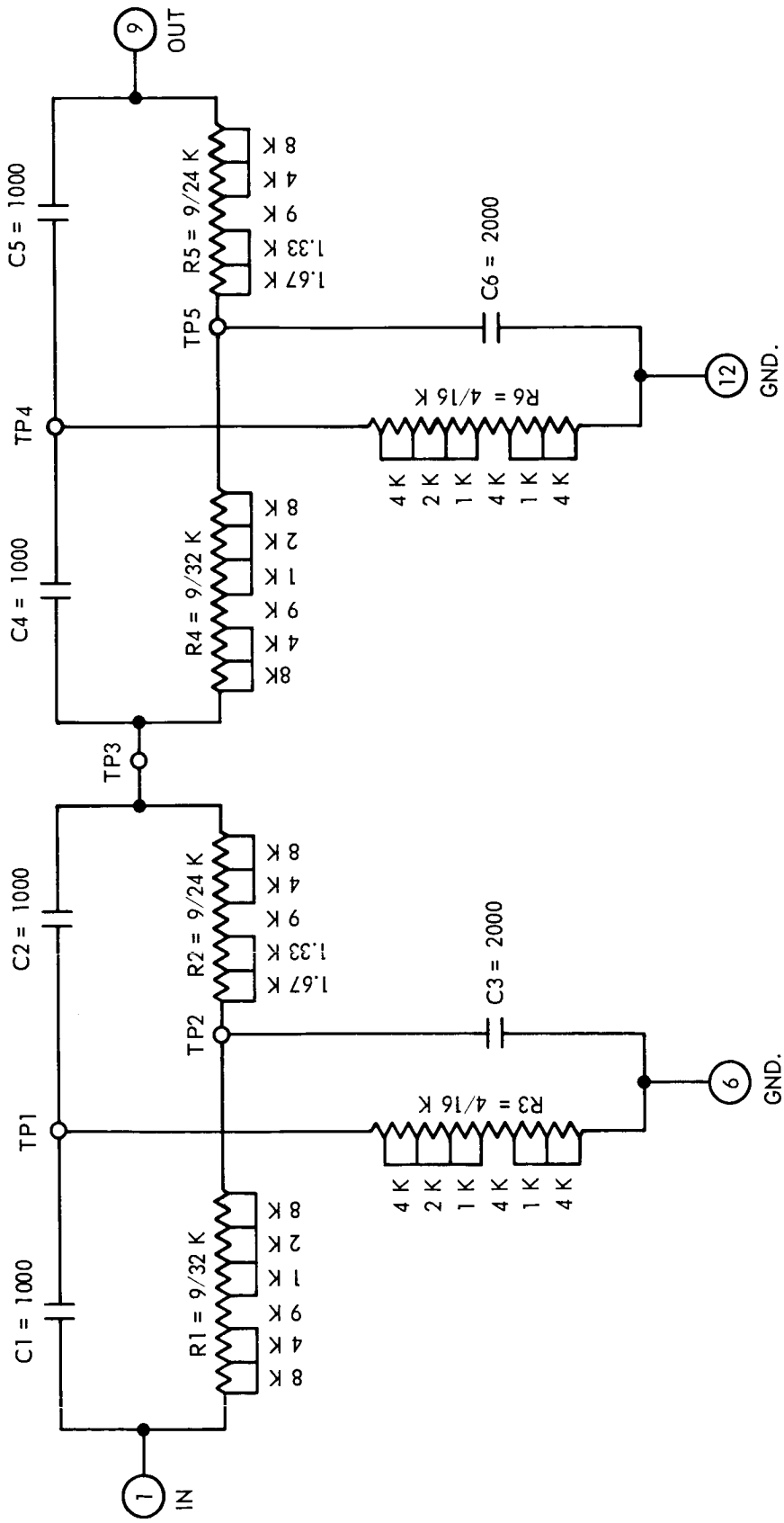


Figure 11. R65018-1 Double Twin T Filter - Schematic

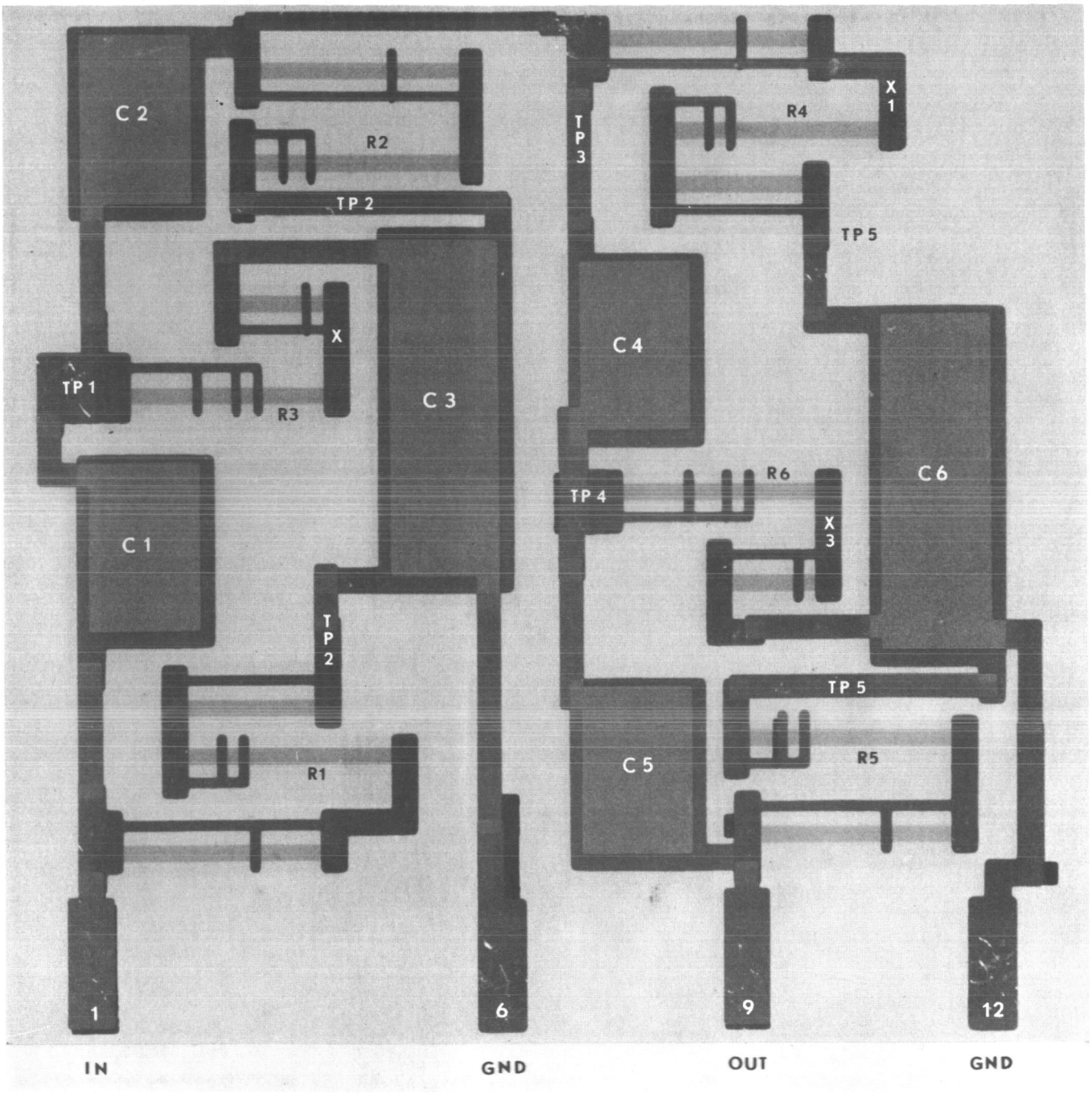


Figure 12. R65018-1 Double Twin T Filter - Substrate

B0367

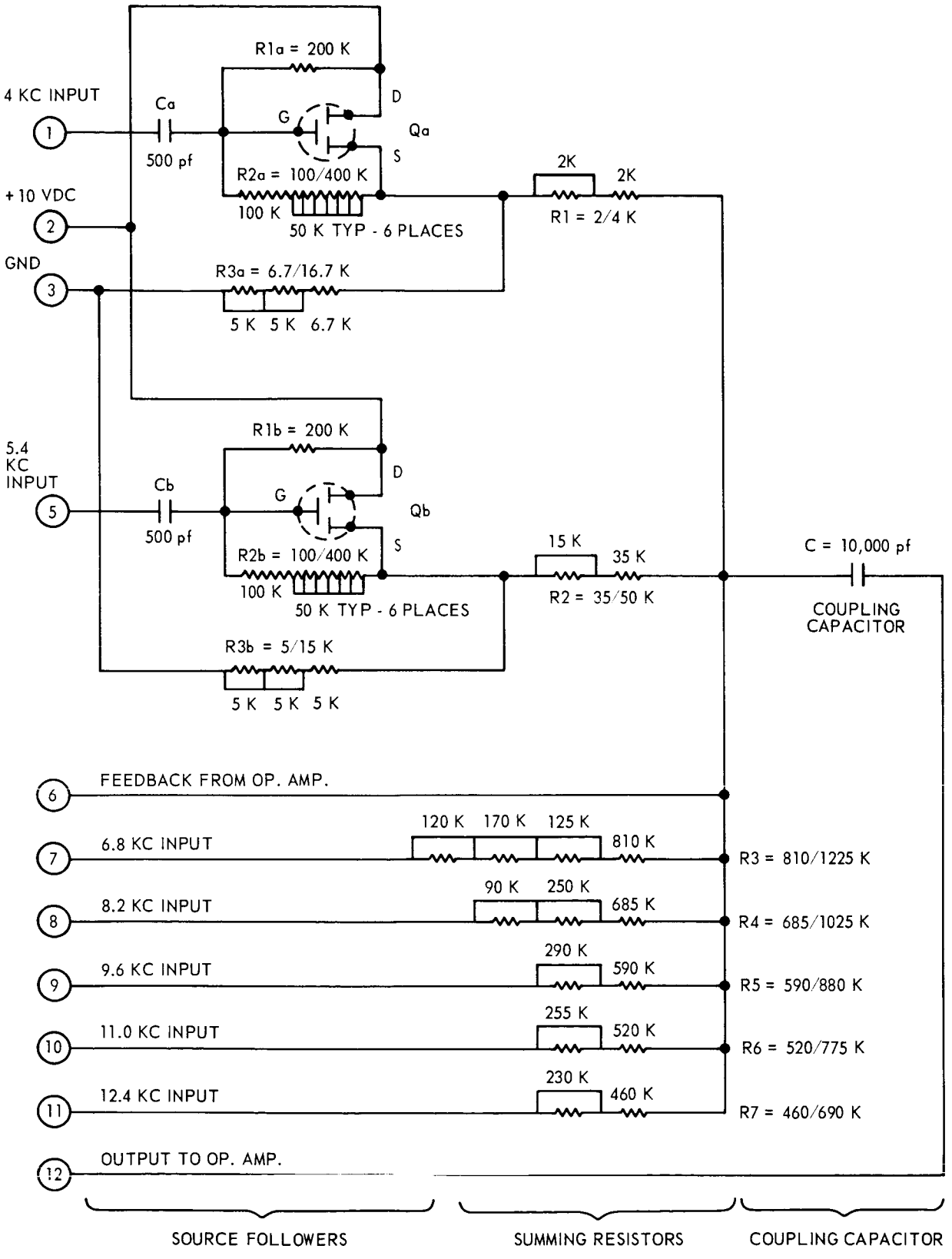


Figure 13. 5006-9 Source Followers, Summing Resistors, and Coupling Capacitor - Schematic

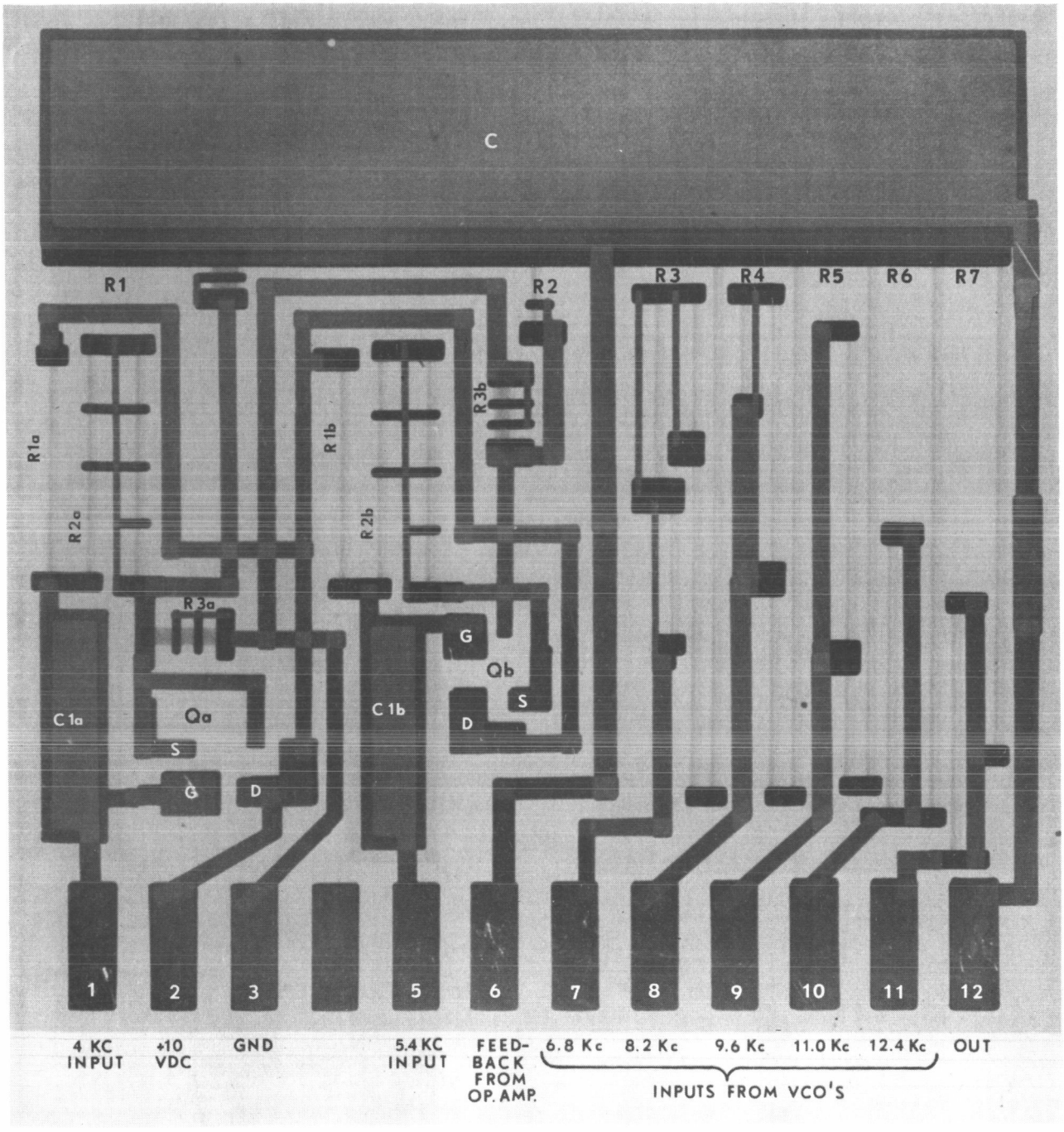


Figure 14. 5006-9 Source Followers, Summing Resistors, and Coupling Capacitor - Substrate

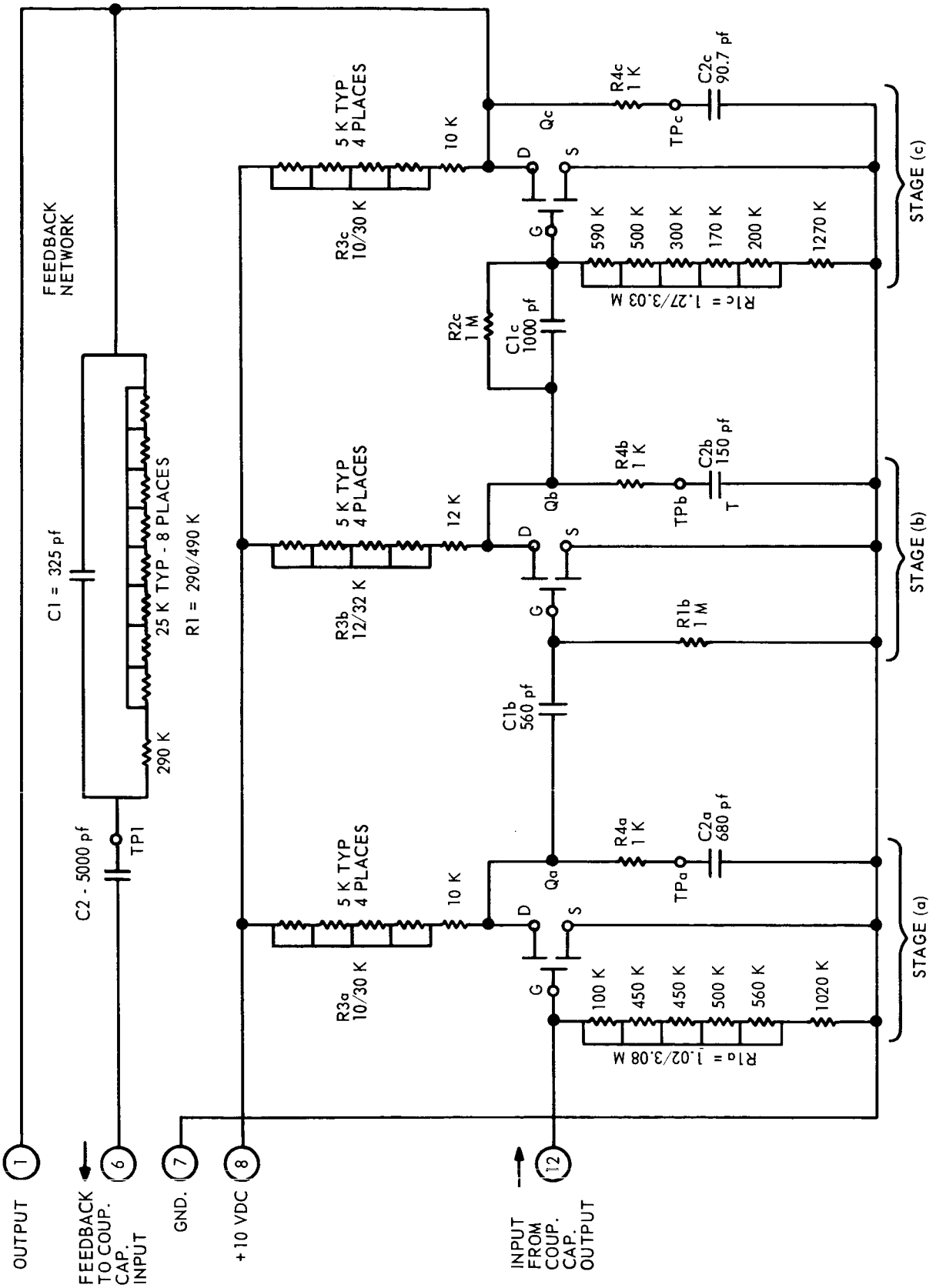


Figure 15. 5006-10 Operational Amplifier - Schematic

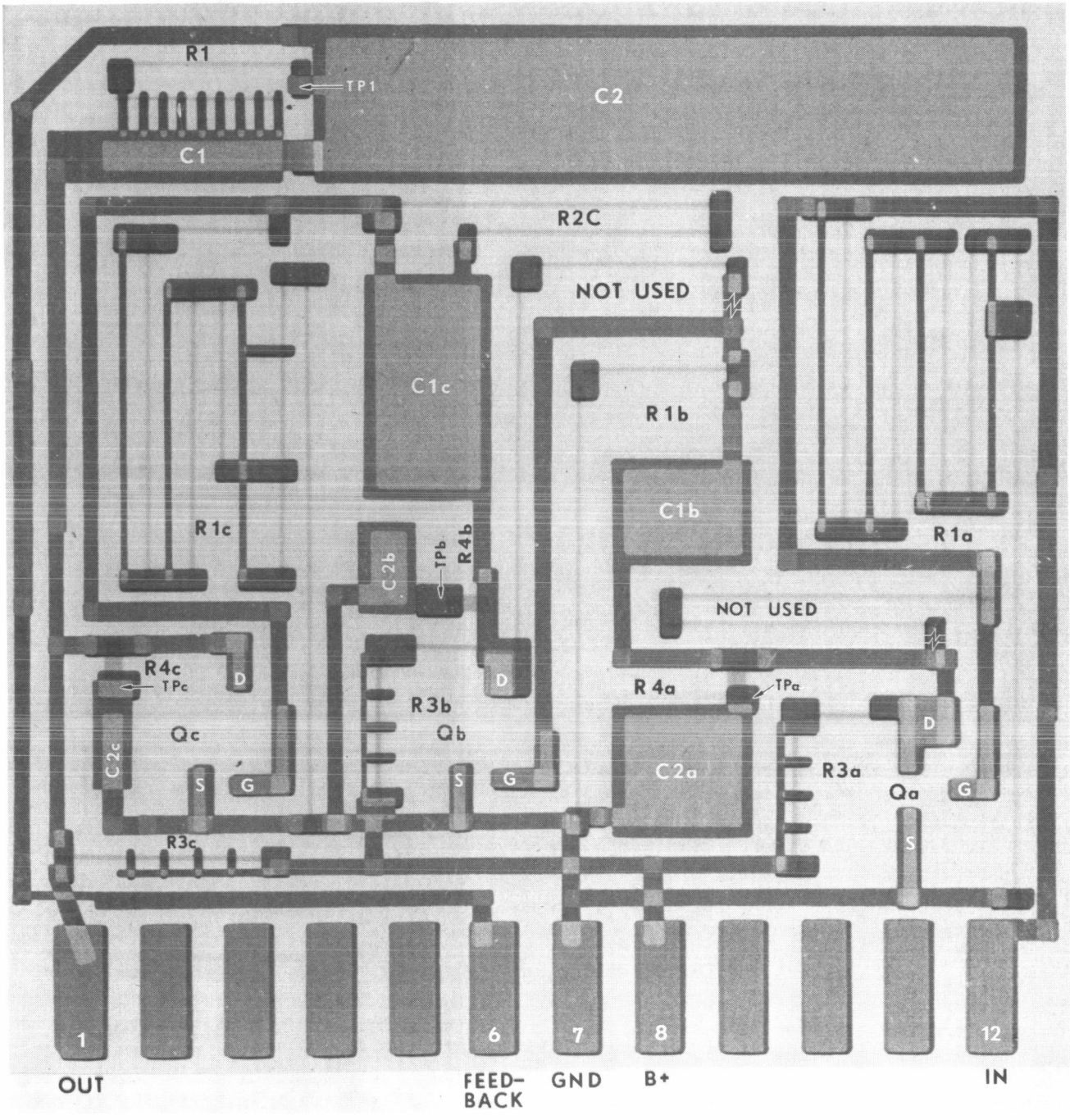


Figure 16. 5006-10 Operational Amplifier - Substrate

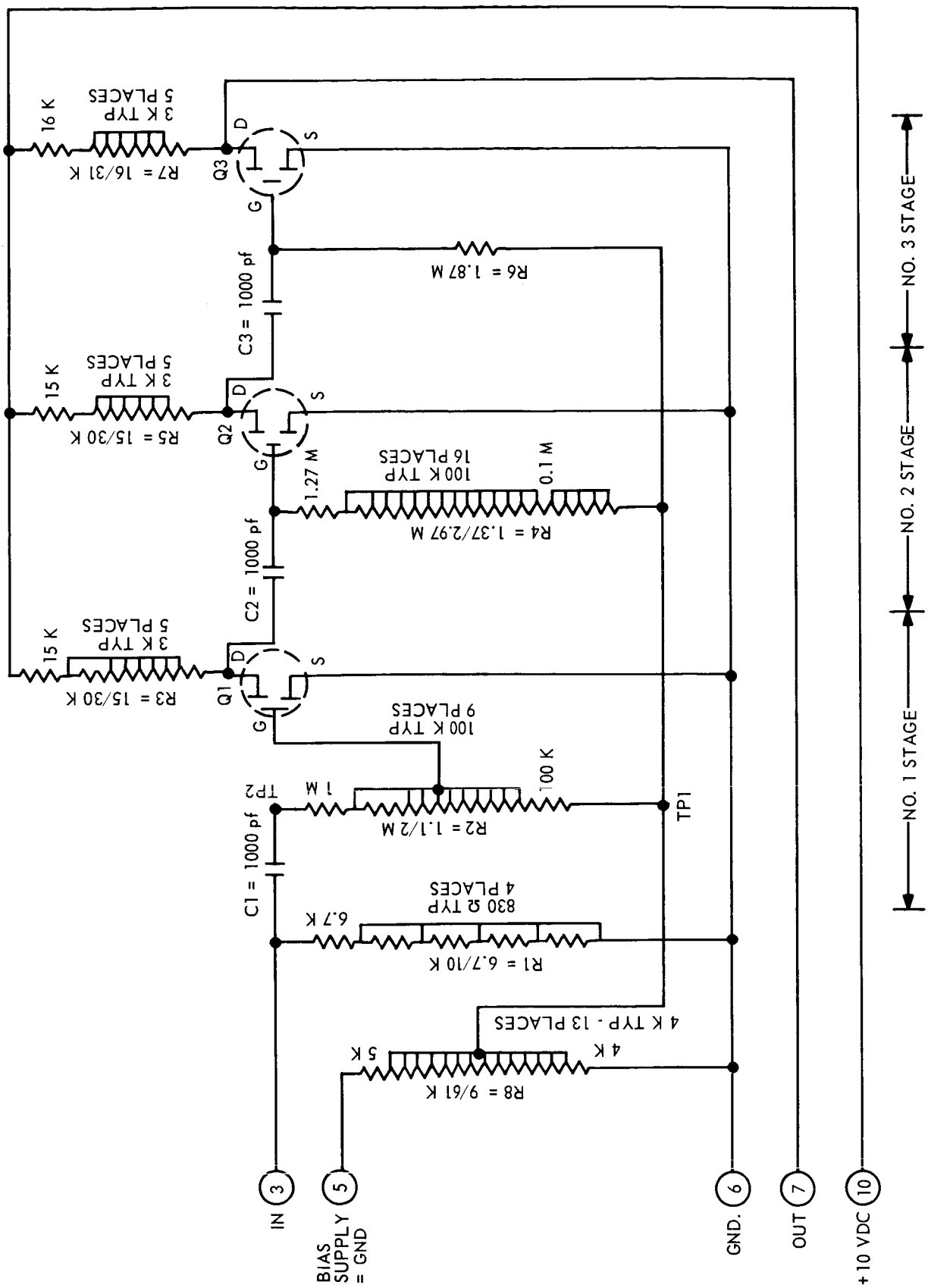


Figure 17. 5006-11 Audio Amplifier - Transmitter - Schematic

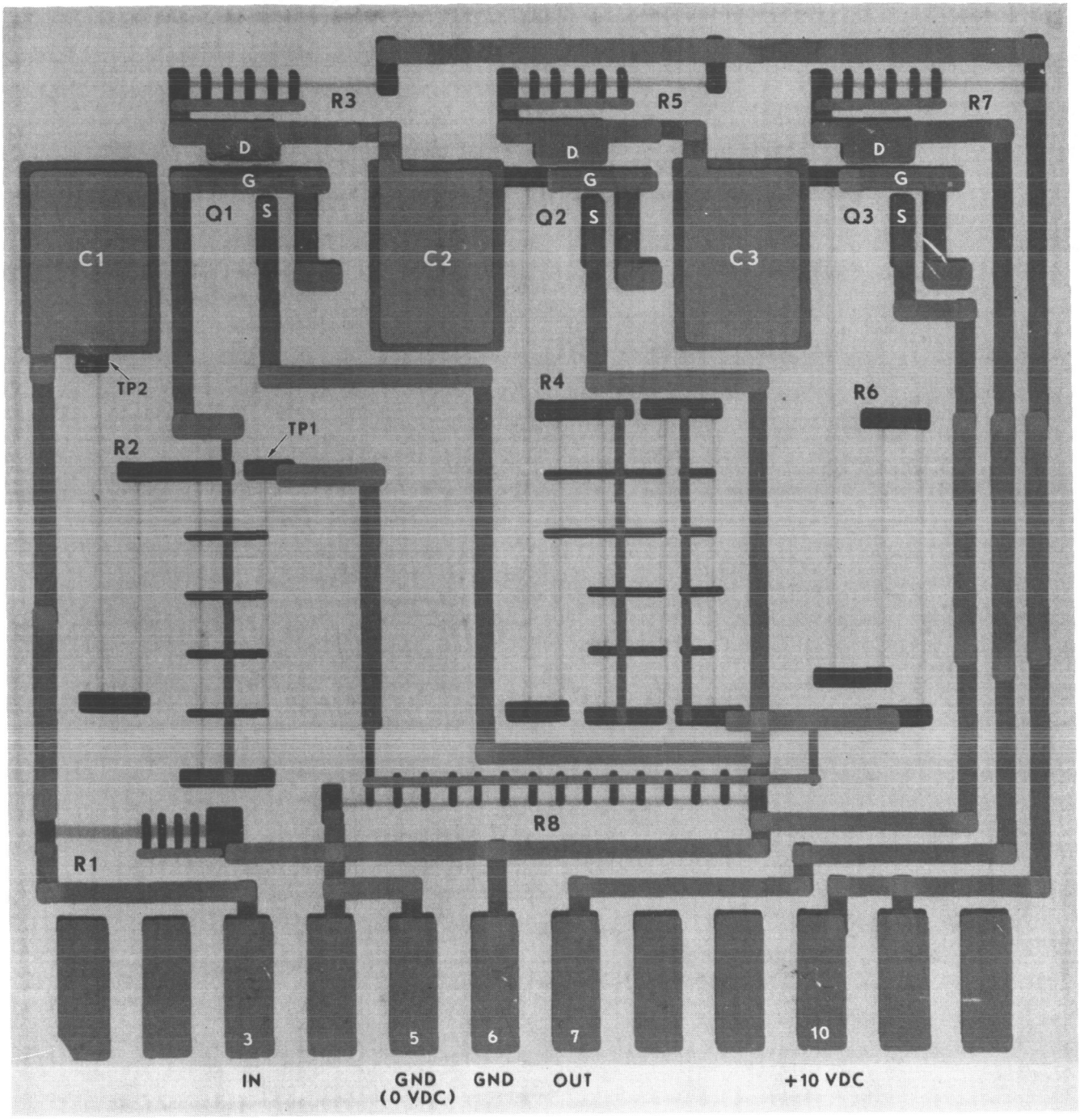


Figure 18. 5006-11 Audio Amplifier - Transmitter - Substrate

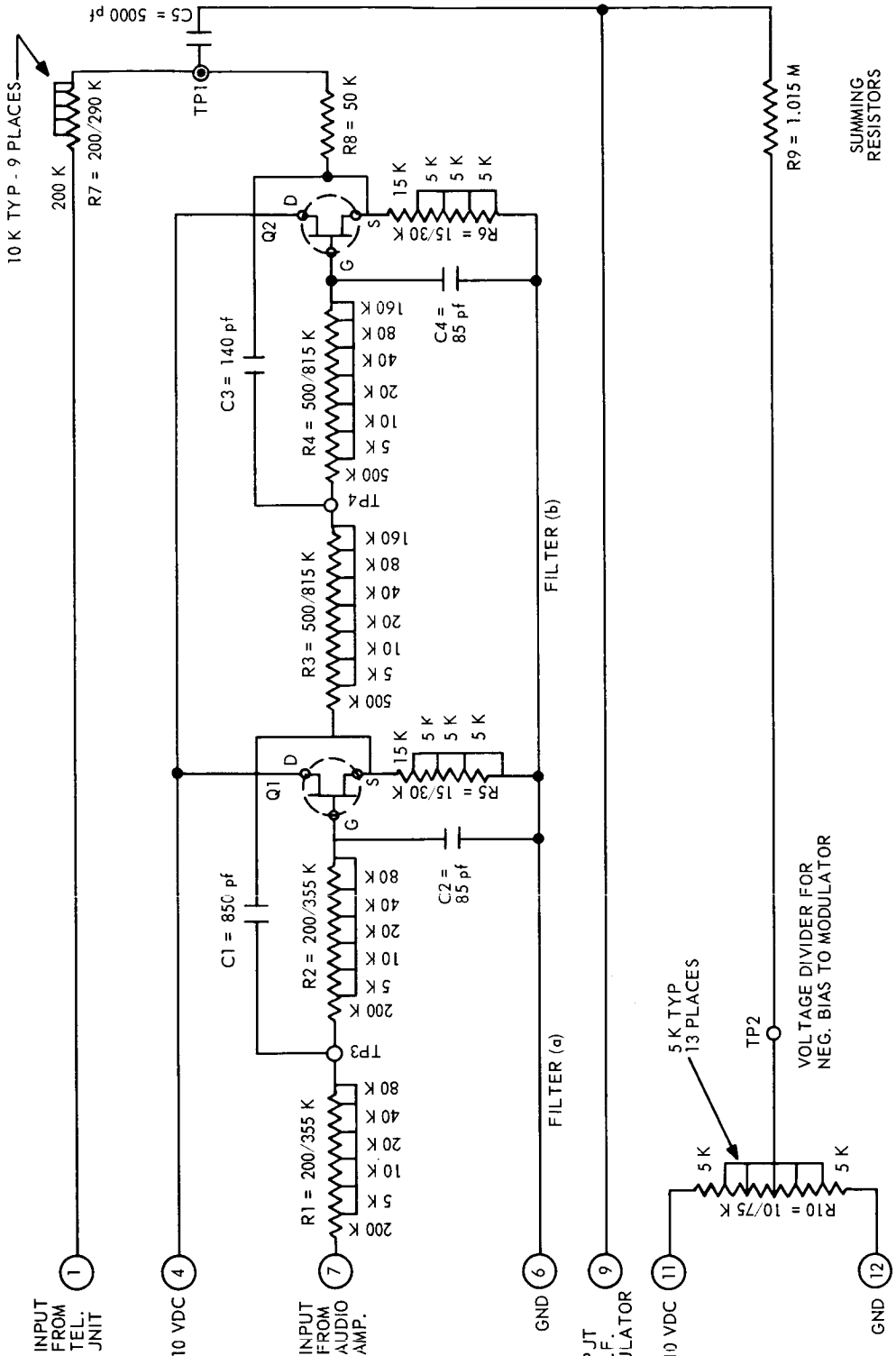


Figure 19. 5006-12 Low Pass Filter, Bias Supply for Modulator, and Summing Resistors - Schematic

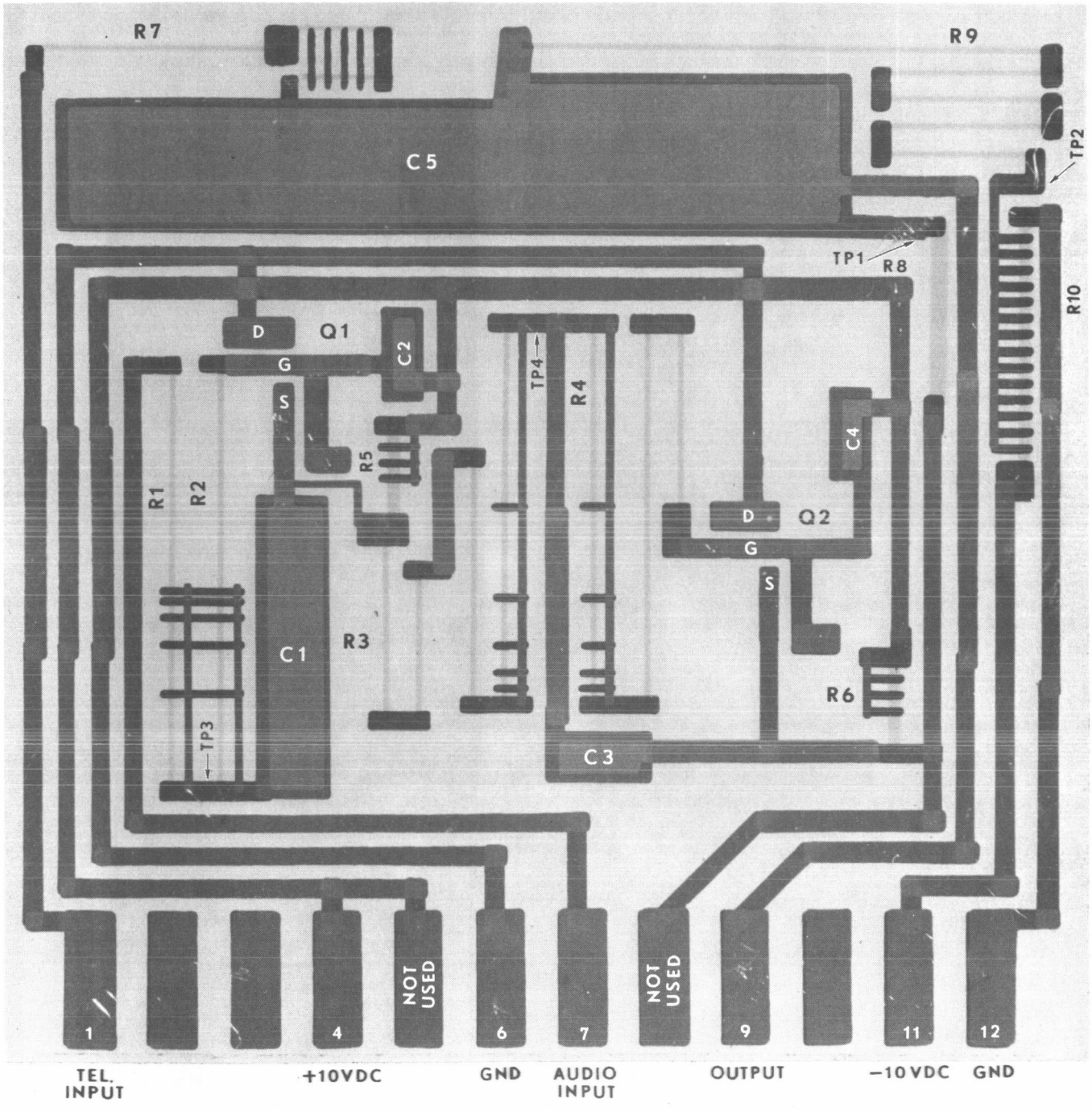


Figure 20. 5006-12 Low Pass Filter, Bias Supply for Modulator, and Summing Resistors - Substrate

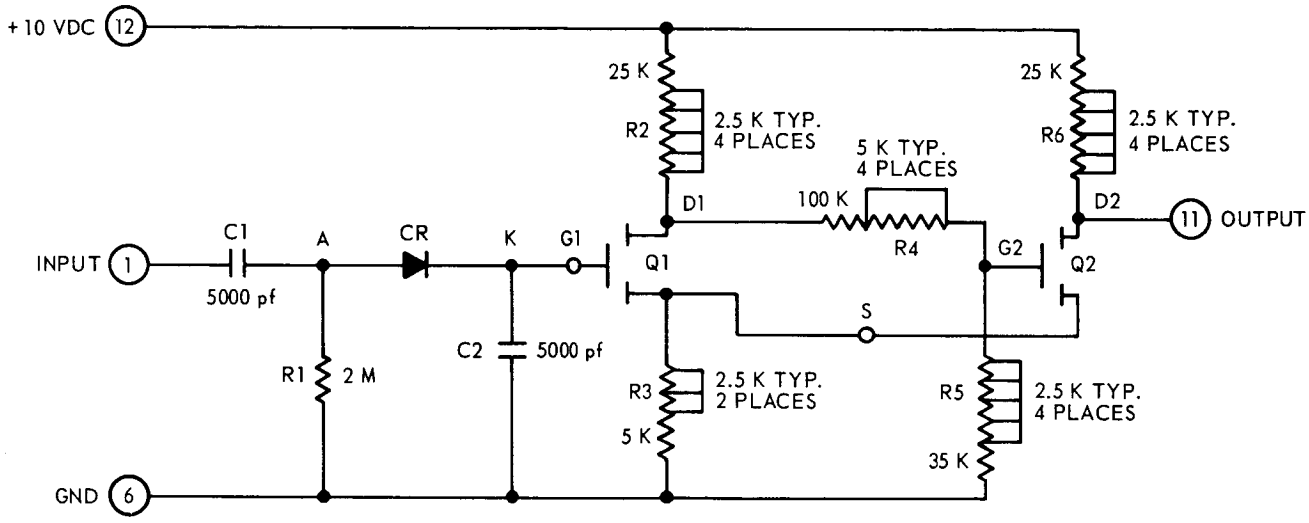


Figure 21. 5006-16 (VOX) Voice Operated Switch - Schematic

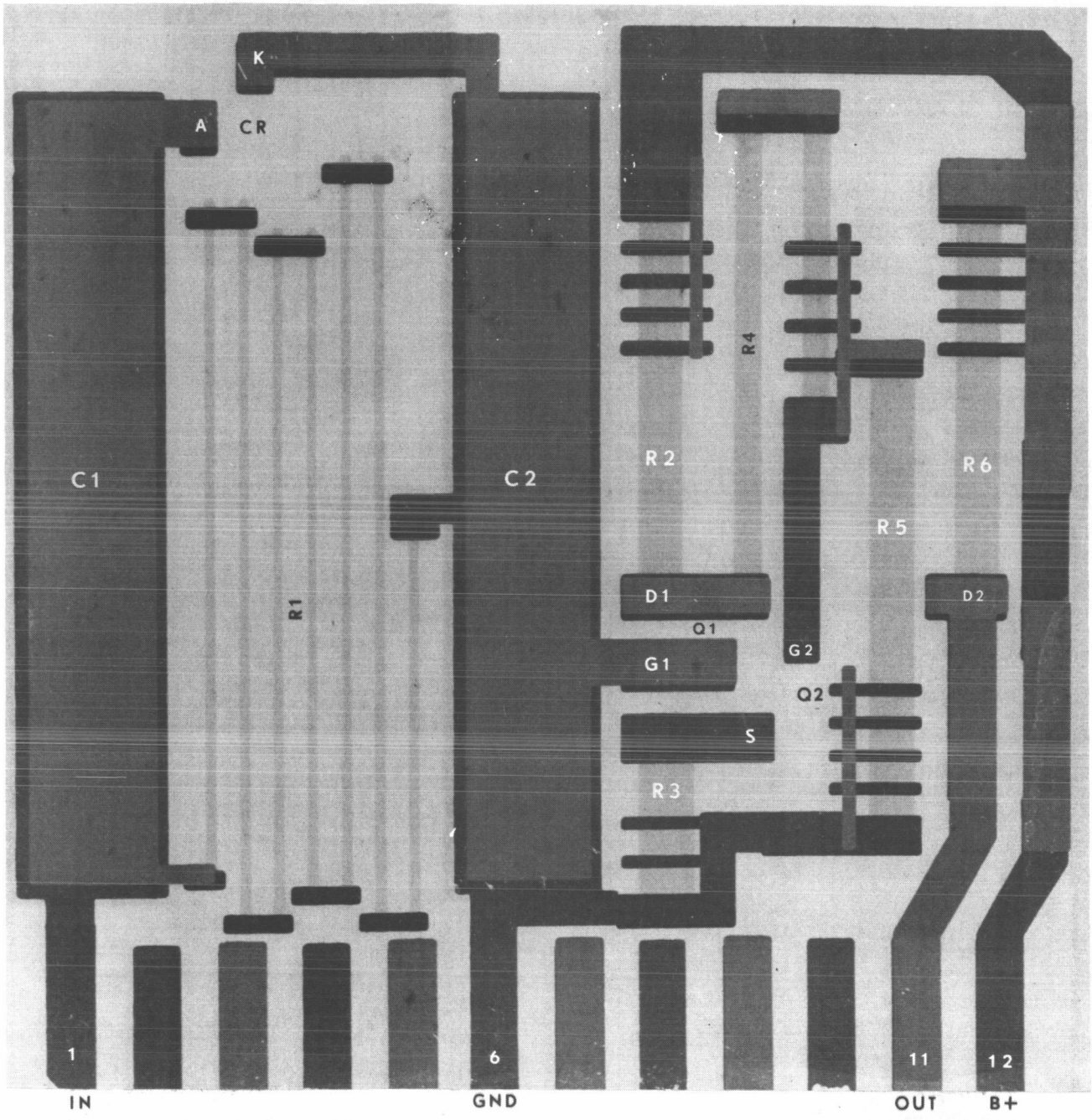


Figure 22. 5006-16 Voice Operated Switch (VOX) - Substrate

FOLDOUT FRAME

5006-13 I.F. AMPLIFIER NO. 1

POST-TRIM RESISTOR VALUES:

I - R^1 = 1 K Ω/□

R2a thru R2g = 10 K (OR LESS) TO 18 K (OR HIGHER) IN 3 K MAX. INCREMENTS

R3b, d, f = 1 K $^{+\ 43.5\%}_{-\ 34.6\%}$

R7 = 100 K $^{+\ 41.2\%}_{-\ 31.0\%}$

R8 = 25 K $^{+\ 42.8\%\ \text{NON-TRIM}}_{-\ 34.6\%\ \text{SEGMENT}}$, WITH 10 TRIM SEGMENTS, EACH = 5 K $^{+\ 51.8\%}_{-\ 36.3\%}$

II - R^1 = 10 K Ω/□

R1a thru R1g = 47 K $^{+\ 210\%}_{-\ 0}$

R1 = 150 K ± 22.3%

R2, 3, 5, 6 = 5 M $^{+\ 200\%}_{-\ 0}$

R4 = 1 M $^{+\ 200\%}_{-\ 0}$

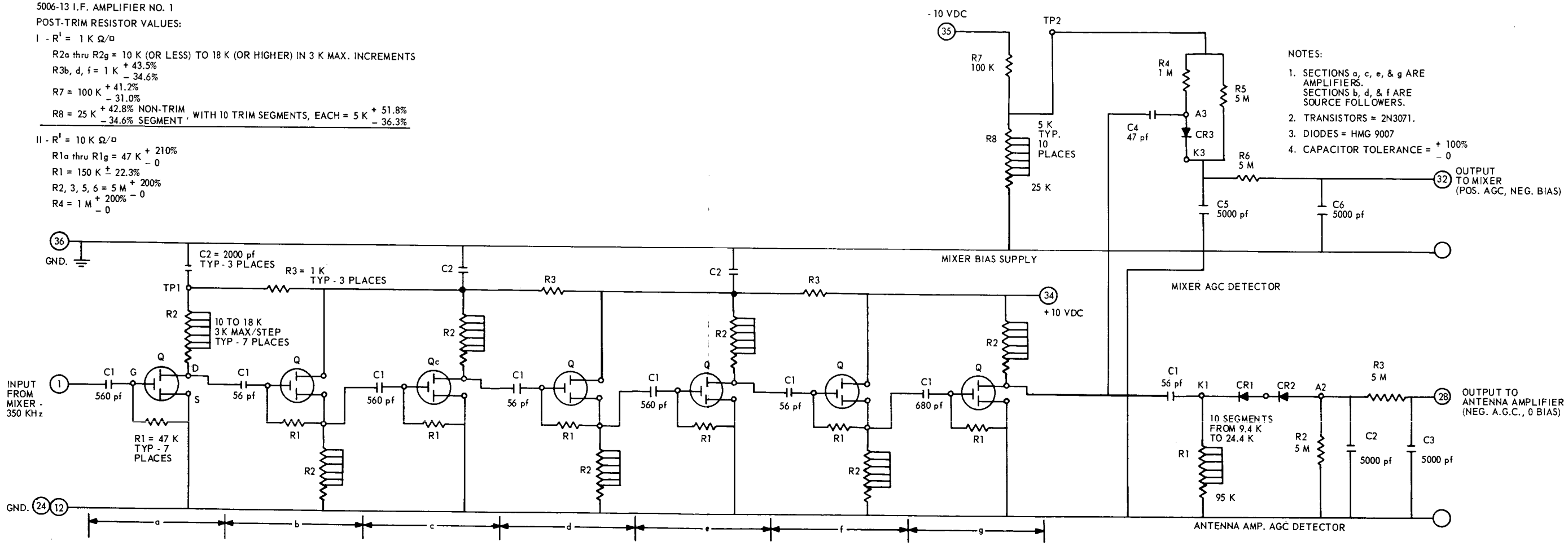


Figure 23. 5006-13 IF Amplifier No. I - Schematic

72-1

FOLDOUT FRAME

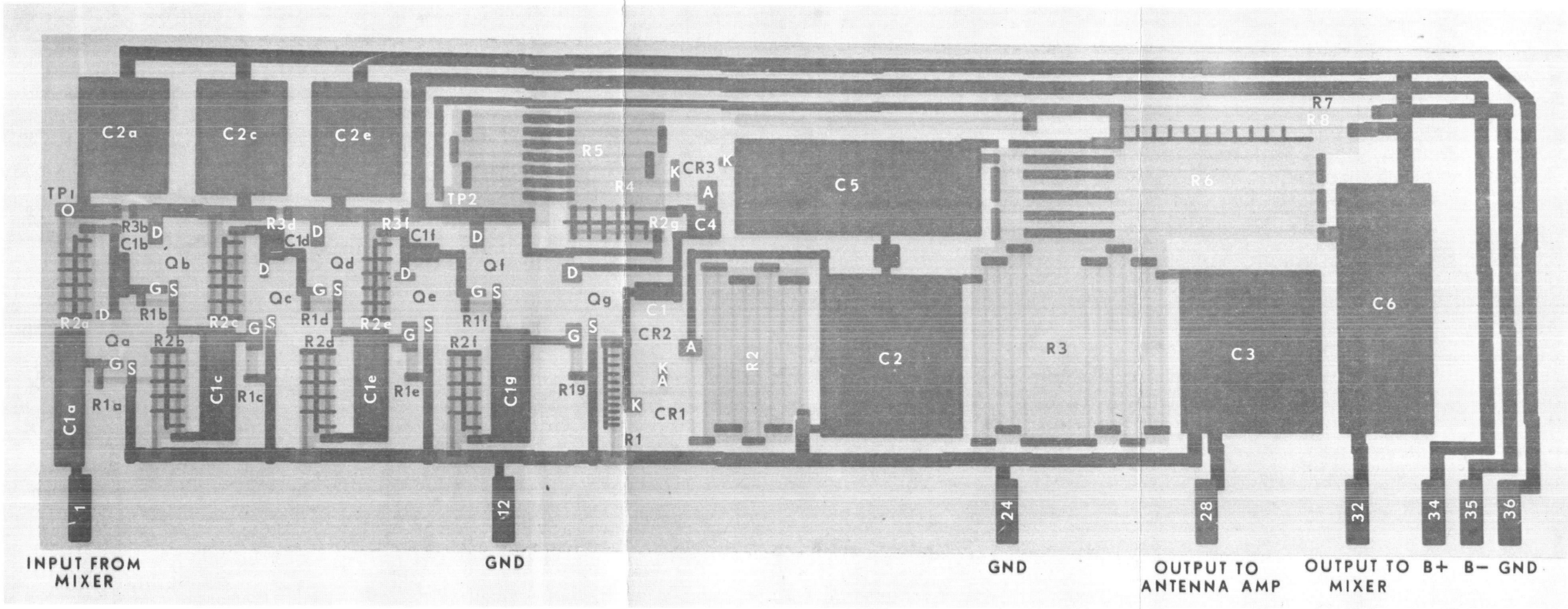


Figure 24. 5006-13 IF Amplifier No. 1 - Substrate

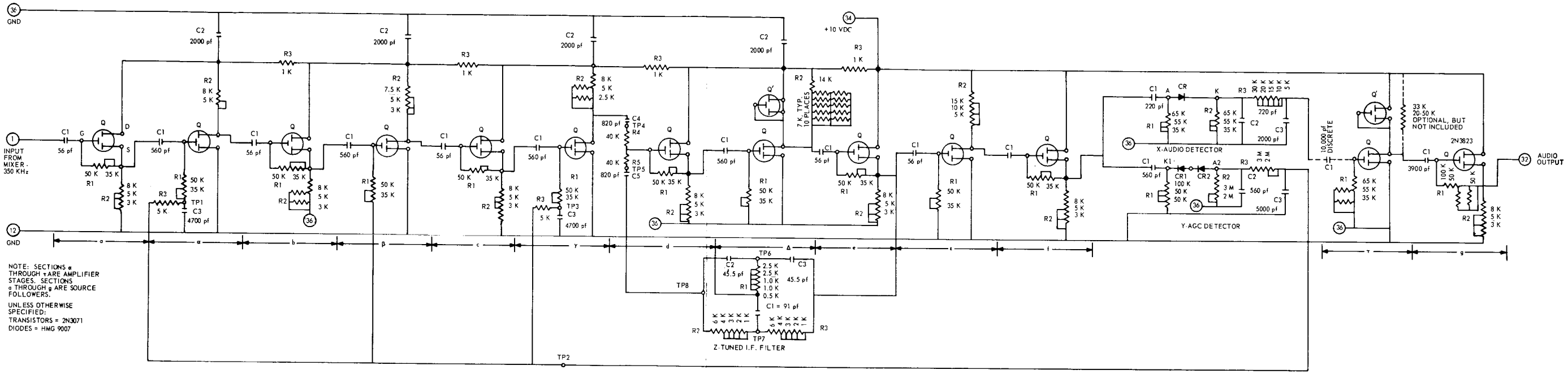


Figure 25. 5006-15 IF Amplifier No. 2 - Schematic

FOLDOUT FRAME

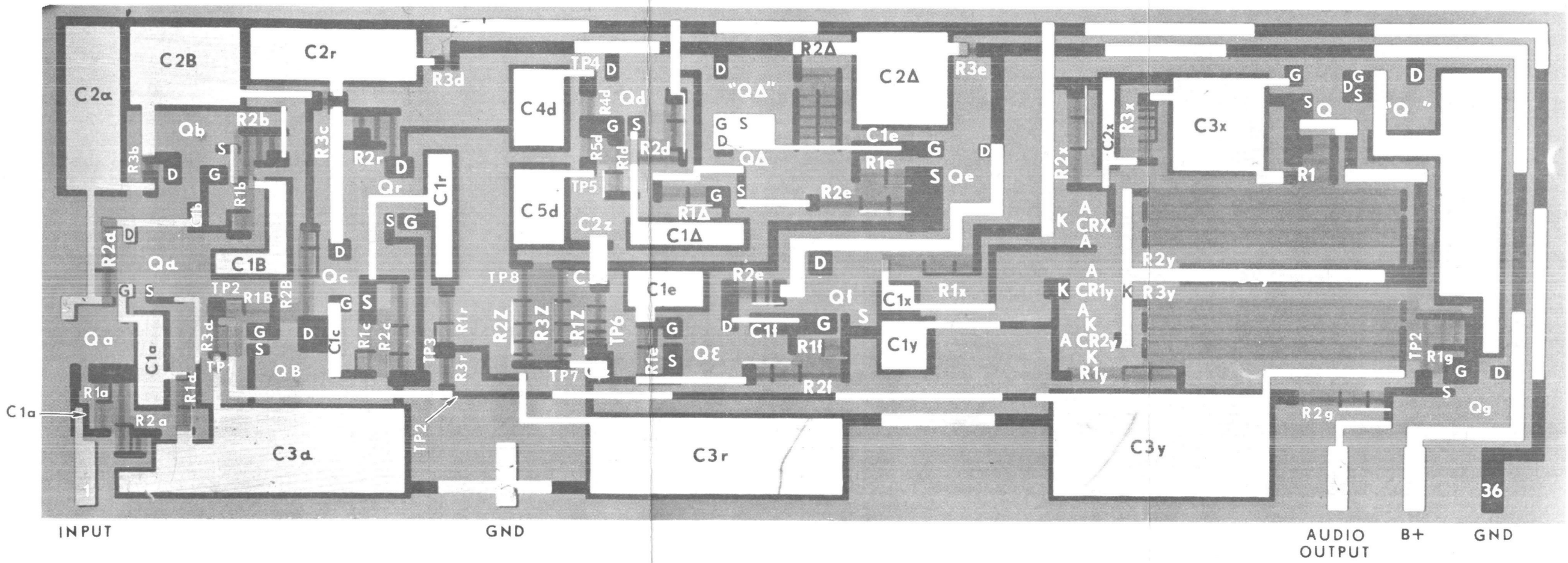


Figure 26. 5006-15 IF Amplifier No. 2 - Substrate

75-1

B0351

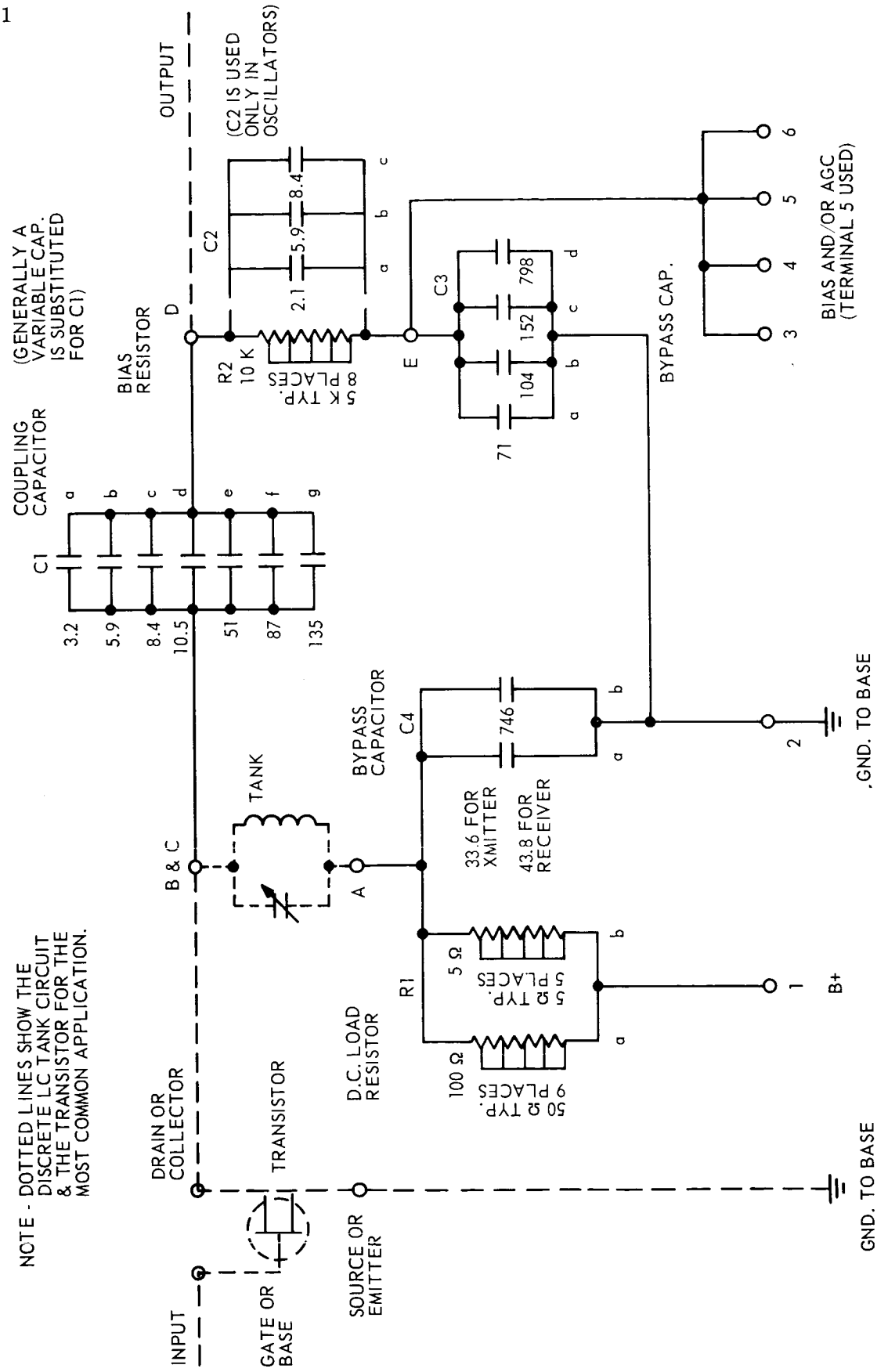


Figure 27. 5006-14 Universal RF Amplifier - Schematic

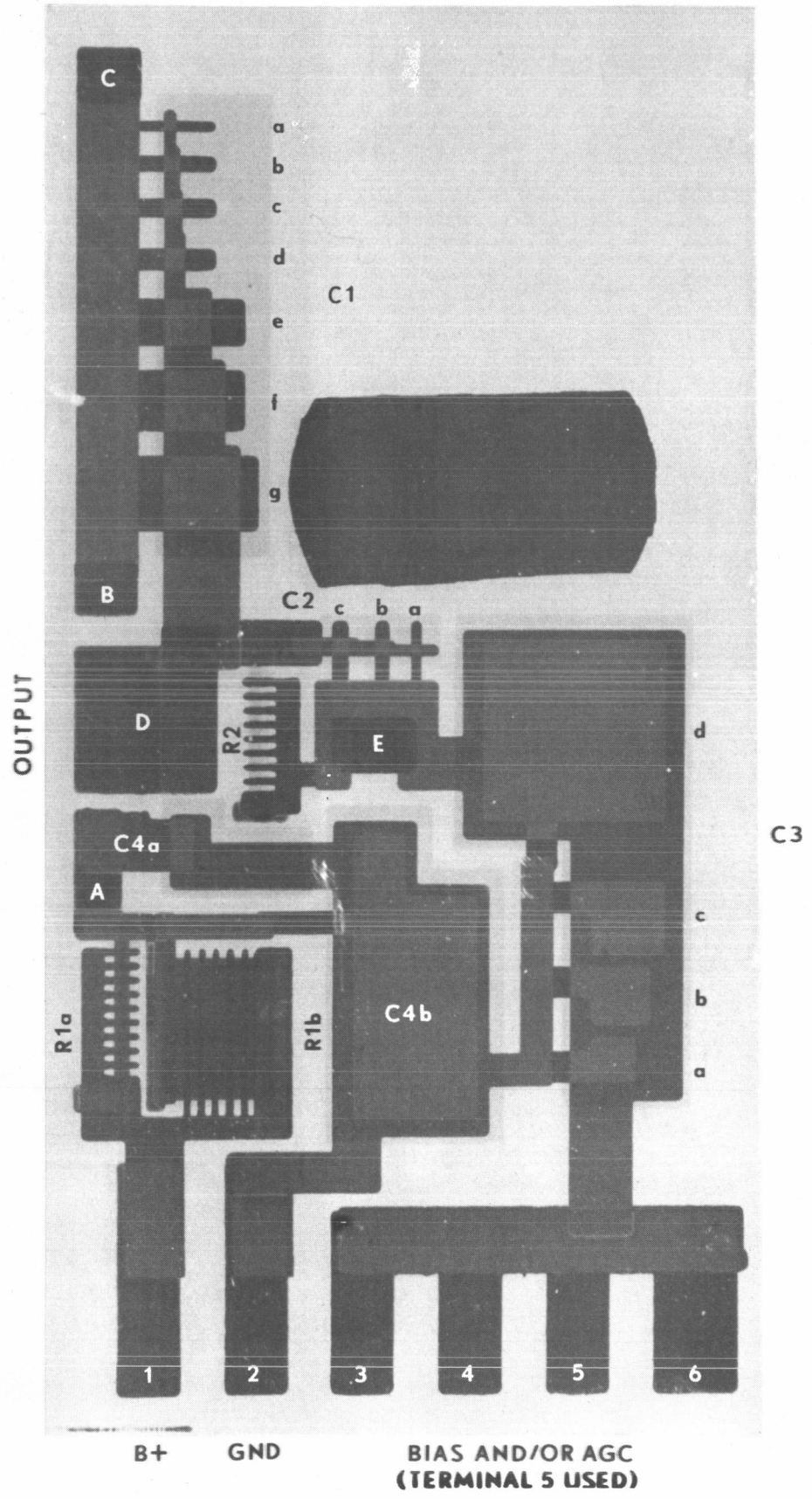


Figure 28. 5006-14 Universal RF Amplifier - Substrate

FOLDOUT FRAME

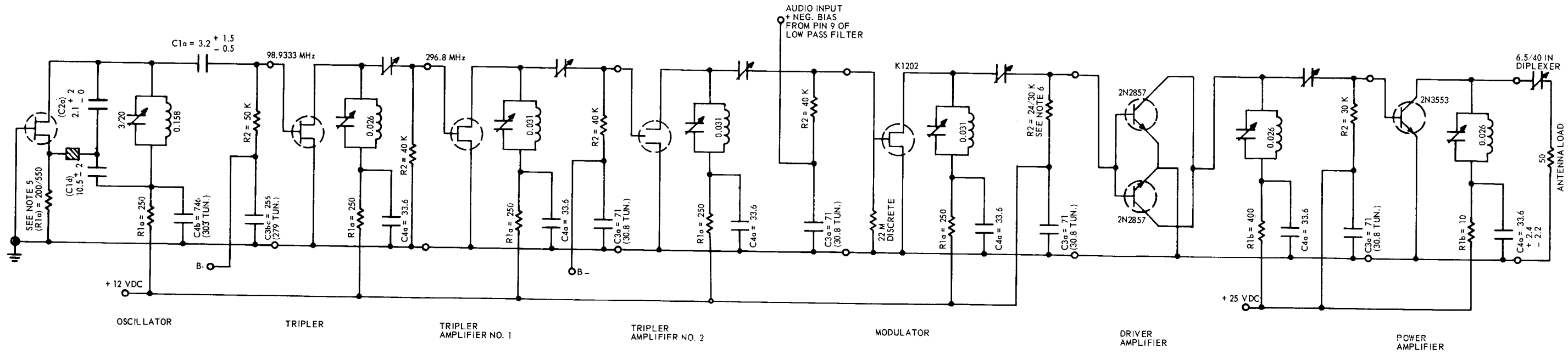


Figure 29. Transmitter RF Portion - Schematic

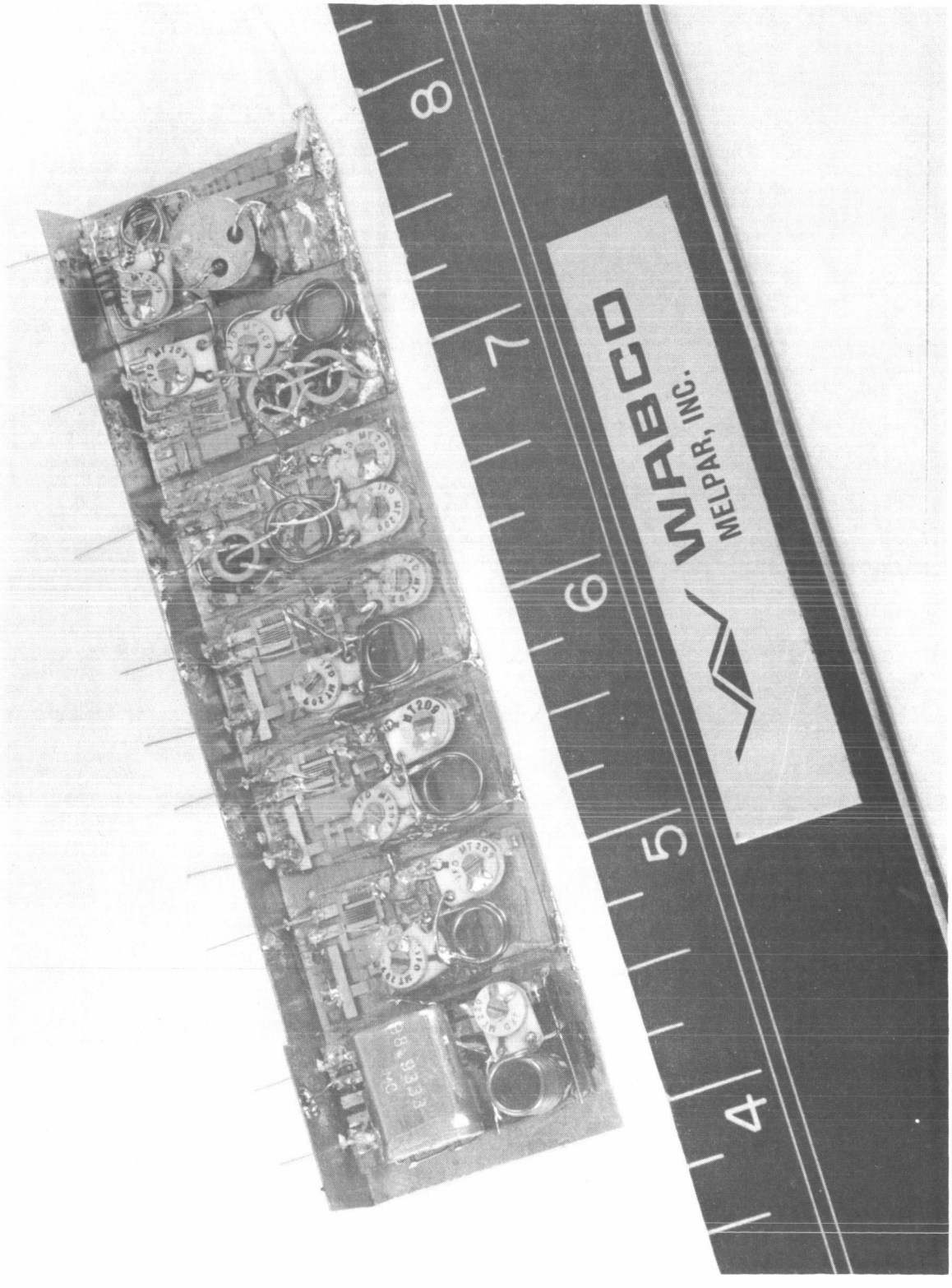


Figure 30. Transmitter, RF Portion with Cover Removed

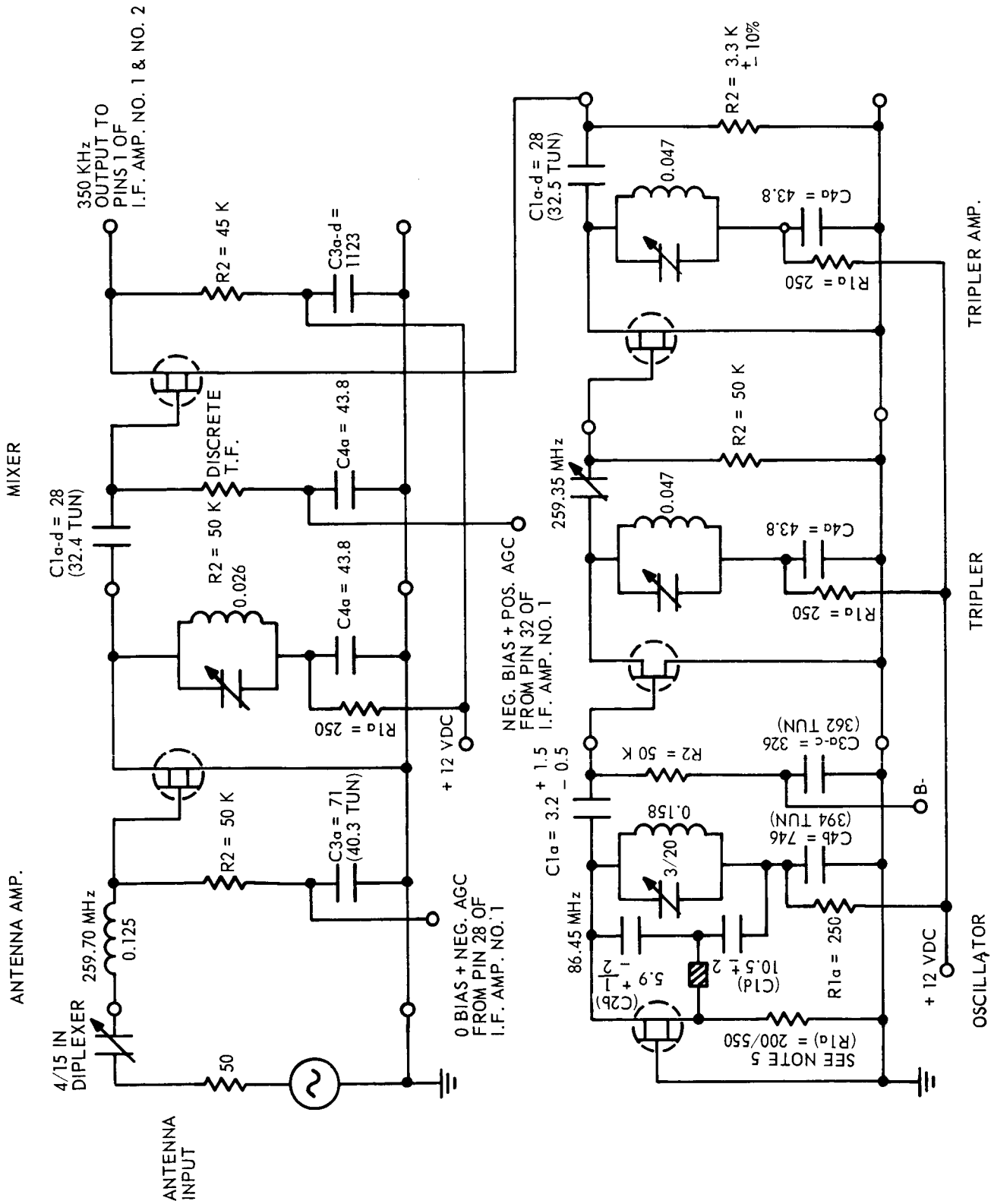


Figure 31. Receiver - RF Portion - Schematic

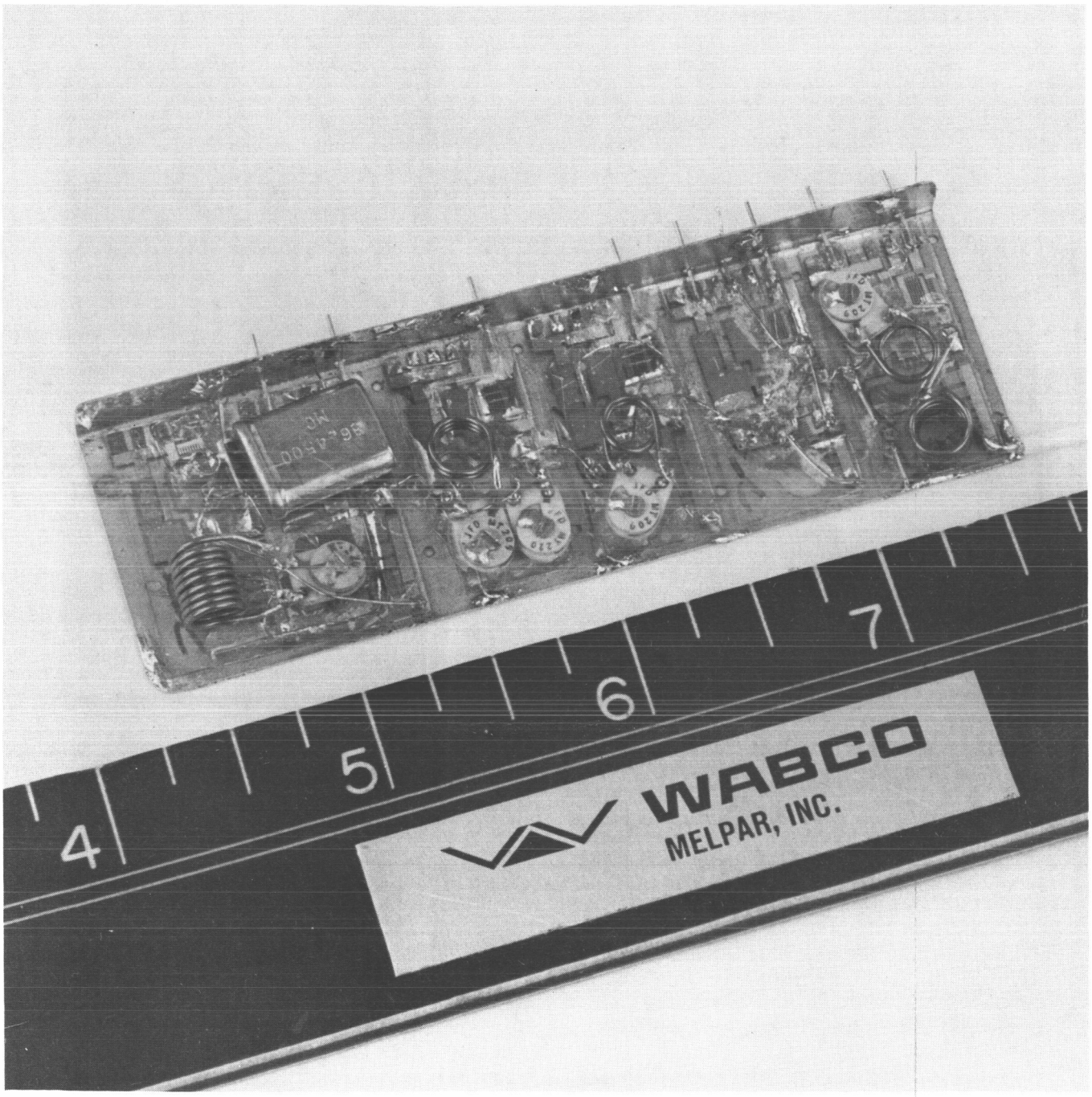


Figure 32. Receiver, RF Portion with Cover Removed

NOTES FOR RF SCHEMATICS

1. Units - Resistors = Ohms

Capacitors = pf

Inductors = uh

2. Unless otherwise specified:

(a) resistor tolerance = ± 20%

(b) capacitor tolerance = ± 12%, except C4a = ± 25%

(c) variable capacitor range = 1.6 to 9 pf

(d) variable capacitors are the MT series, manufactured by JFD Electronics Company, Brooklyn, New York.

(e) transistors are 2N3823 in chip form

(f) oscillator crystals are quartz, CR-56A/U (MIL-C-3098/34B)

3. For receiver oscillators (R1), (C1), (C2), are located in the right hand circuit and R1, R2, C3 and C4 are located in the left hand circuit of a 1" x 1" substrate.

4. Transmitter oscillators are composed of two 1" x 0.5" circuits mounted back-to-back with the film sides facing away from each other. (R1), (C1), and (C2) are on the lower substrate and R1, R2, C3, and C4 are on the upper substrate.

5. For oscillators, the source resistor, (R1), is trimmed under test, from a minimum of 200 ohms to a maximum of 550 ohms in 50 ohm steps, until oscillation commences. (At each value of resistance, the tank capacitor is slowly adjusted through its entire range to determine whether or not oscillation will occur.)

6. For the driver amplifier, the bias resistor, R2, is trimmed to a value between 24K and 30K such that the sum of the collector currents for the two parallel transistors is equal to 35 ± 2 ma. This is accomplished by calculating the dc collector voltage as a function of the dc load resistor, 400 ohms ± 20%, and the above current and then trimming the bias resistor up until the collector voltage rises to the calculated value, which is nominally 11Vdc. A high quiescent collector current is required in order to obtain a large amplitude output voltage, due to the low ac load impedance. The 37 ma limit is imposed so that the maximum current rating of 20 ma per transistor is not exceeded. The power dissipation per transistor is about 193 mW, which is safe at an ambient air temperature up to 50°C, due to the fact that the transistor cases are soldered to the brass base plate of the RF section. The temperature gradient between the transistor cases and the ambient air is less than 15°C.

7. Negative bias for the transmitter modulator is that value which reduces the unmodulated output voltage across the antenna load to one half of its maximum value. The maximum value is first determined by varying the modulator bias and then the bias is further adjusted until half of the above output voltage is obtained.

All other negative biases, for both transmitters and receivers, are those values which yield maximum output voltage. All biases were determined using variable dc supplies. Negative biases

for the transmitter modulator and receiver mixer are supplied from trimmable, thin film voltage dividers located on the "Low Pass Filter" and the "I.F. Amplifier No. 1", substrates, respectively. All other negative biases are supplied from voltage dividers composed of 1/8 watt, discrete resistors located on the mother P.C. board.

Typical biases are listed below:

Tripler (Transmitter + Receiver)	- 7 Vdc
Tripler Amplifier No. 2 (transmitter)	- 0 Vdc
Modulator (transmitter)	- 2 Vdc
Mixer (Receiver)	- 3 Vdc

8. It is desirable that all fixed capacitors have low impedance except the divider network and coupling capacitor in the oscillators (C1d), (C2a), and C1a.

All other fixed capacitors have their tuned value specified, unless the tuned value is not provided in the thin film circuit, in which case the closest available capacitance is specified and the tuned value designated "tun", is listed for reference.

The tuned value is that value of capacitance which results in zero reactance at the operating frequency when in series with the lead inductance, including both thin film and wire conductors.

The lead inductance for each thin film capacitor, with typical wire leads connected, was determined by finding the resonant frequency (at which impedance is minimum) and then by calculating inductance as a function of capacitance and resonant frequency.

It was necessary to reduce the area of C4a in order to tune out the lead inductance for low bypass impedances at 259.7 and 296.8 MHz. This was accomplished by spot welding pieces of .003" thick tantalum to the small capacitor plate mask. The correct capacitances are fabricated to an accuracy of ± 25% (including ± 8% for variation in C/A from batch to batch) on 11 circuits for each frequency. These are:

Transmitter - 296.8 MHz, C = 33.6 pf + 25%

1a & b, 3a & b, 4a, 5b, 6a, 11b, 13a, 14a & b

Receiver - 259.7 MHz, C = 43.8 pf + 25%

4b, 5a, 9a, 10a & b, 11a, 13b, 15a & b, 16a & b

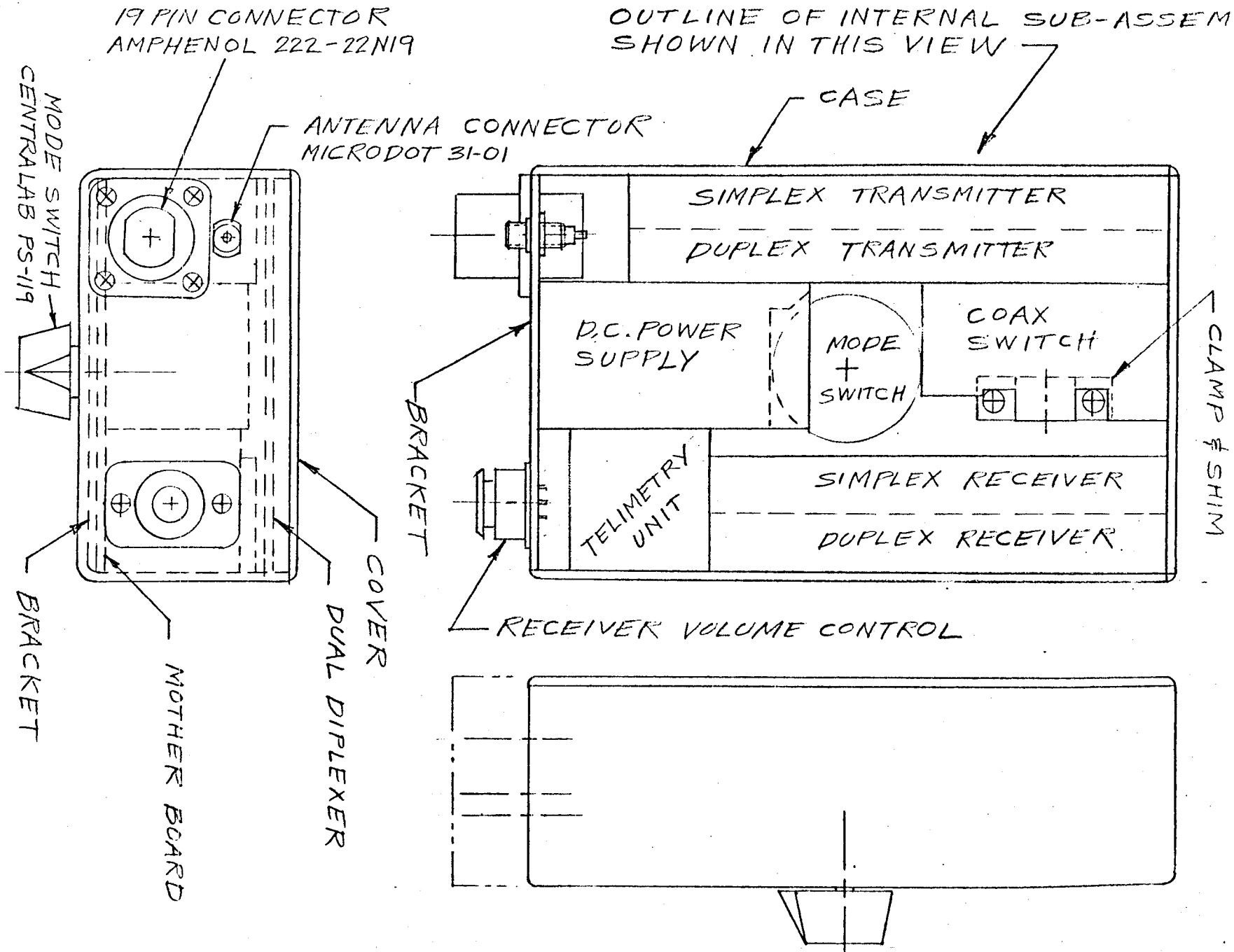
Capacitor C4a on circuits 6b, 7a&b, and 9b, is too low or too high for the above frequencies, but these circuits may be used for oscillators, since C4a is not used in the oscillators.

The ± 25% tolerance is permissible for all stages, except the transmitter power amplifier for which C4a must equal $33.6\ ^{+2.4}_{-2.2}$ pf. With this tolerance, the reactance should not exceed 0.5 ohm, and, with 1 ohm lead resistance, the impedance should not exceed 1.12 ohms which is 11.2% of the 10 ohm load resistor. All other load resistors are 250 or 400 ohms ± 20% and the maximum impedance

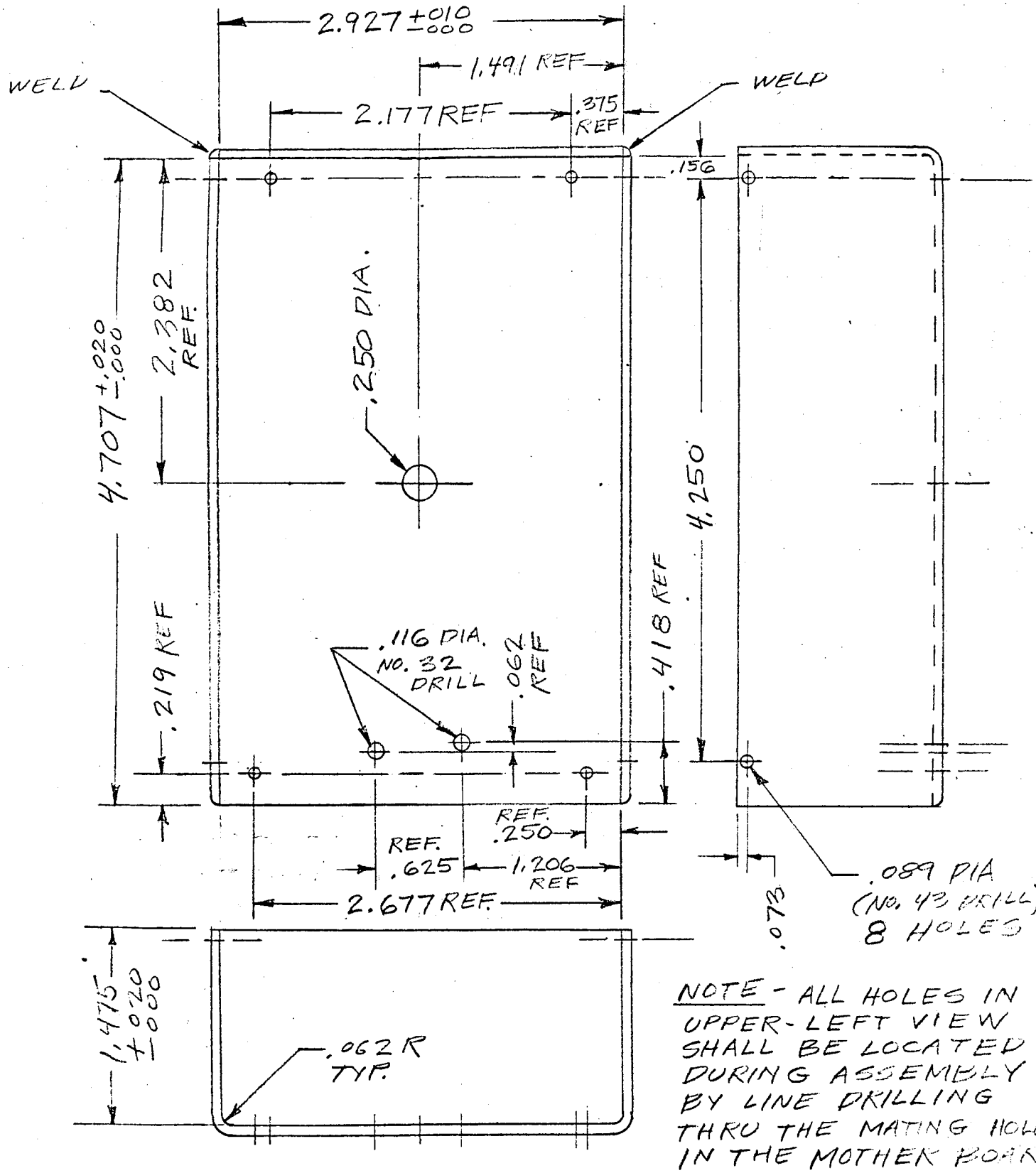
of the bypass capacitor, with a ± 25% tolerance, is about 5 ohms, thus the bypass impedance is only about 2% of the load impedance. It is important that the bypass impedance be a small percentage of the dc load resistance so that the amplitude of any ac voltage fed back to previous stages through the B+ conductor is small enough to prevent instability or self-induced oscillation. It is noted that there are generally at least six circuits per batch in which C4a can meet the power amplifier requirement.

9. All coils are wound using #22 (.025" dia.) varnish coated, copper wire. The inside diameter is 0.175" for all coils except the .031μh coil, for which the inside diameter is 0.200". The number of turns for each coil are 1.5, 1.5, 2.5, 5.0, and 6.5 for inductances of .026, .031, .047, 0.111, and 0.158 microhenrys, respectively.

10. For driver and power amplifiers, the unused portion of the substrate is cut off to allow for heat sinking the transistors to the brass base. The grounded cases of the two 2N2857 transistors in the driver amplifier are soldered to the base. The case of the 2N3553 transistor in the power amplifier may not be grounded, therefore thermal conduction to the base is accomplished by placing a .010 x .333 x .333 piece of berylia between the transistor case and the base, using thermal conducting-electrical insulating epoxy cement to fasten the parts in place.



SKETCH-1 PERSONAL COMMUNICATION AND TELIMETRY SYSTEM (TRANSCEIVER)

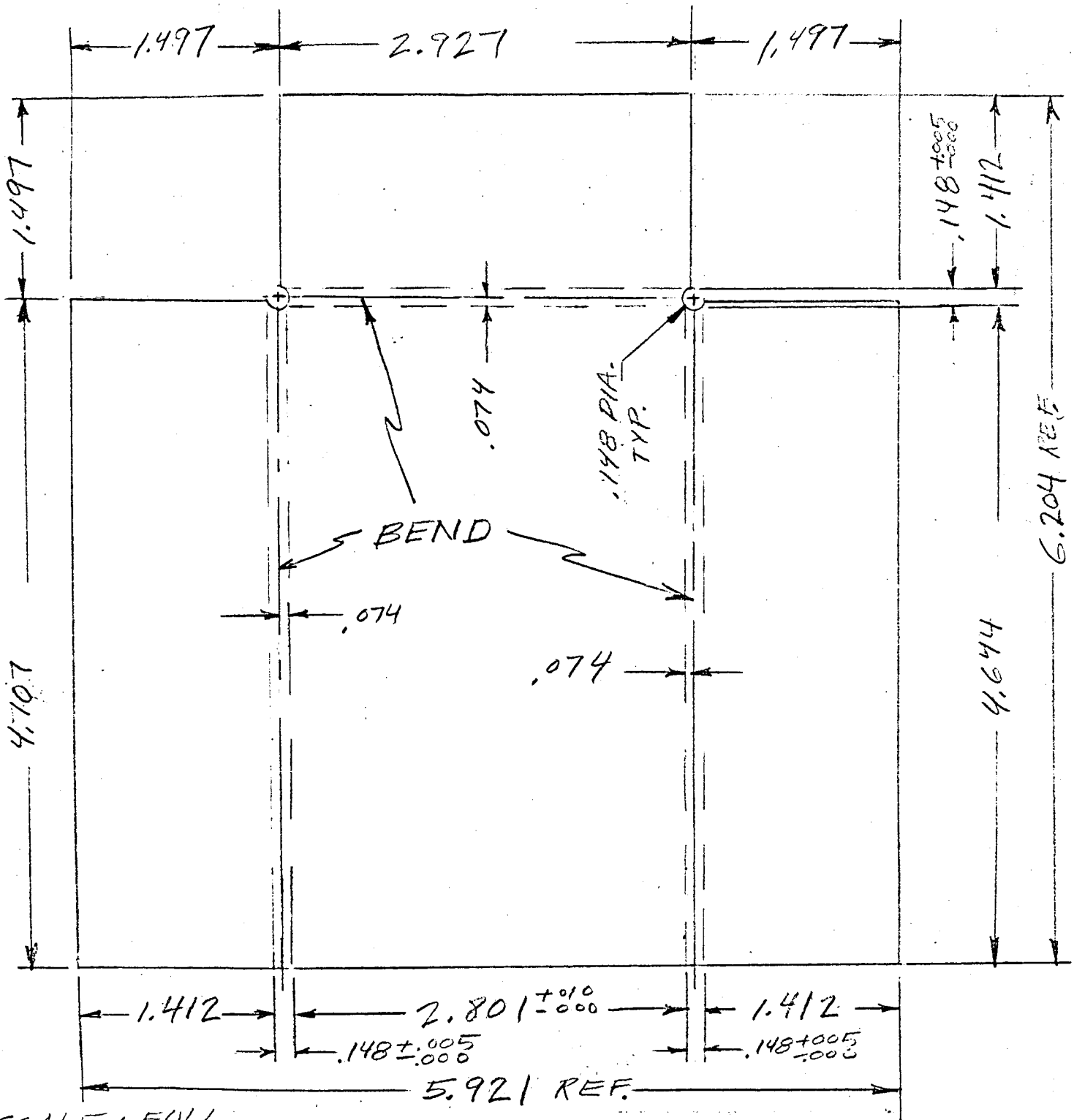


NOTE - ALL HOLES IN UPPER-LEFT VIEW SHALL BE LOCATED DURING ASSEMBLY BY LINE DRILLING THRU THE MATING HOLES IN THE MOTHER BOARD, SKETCH 5. (7 HOLES)

TOL ±.010
MAT'L - ALUM. ALLOY 5052 H32
.062 ± .002 THK.

SCALE: FULL

CASE - TRANSCEIVER
SKETCH-2



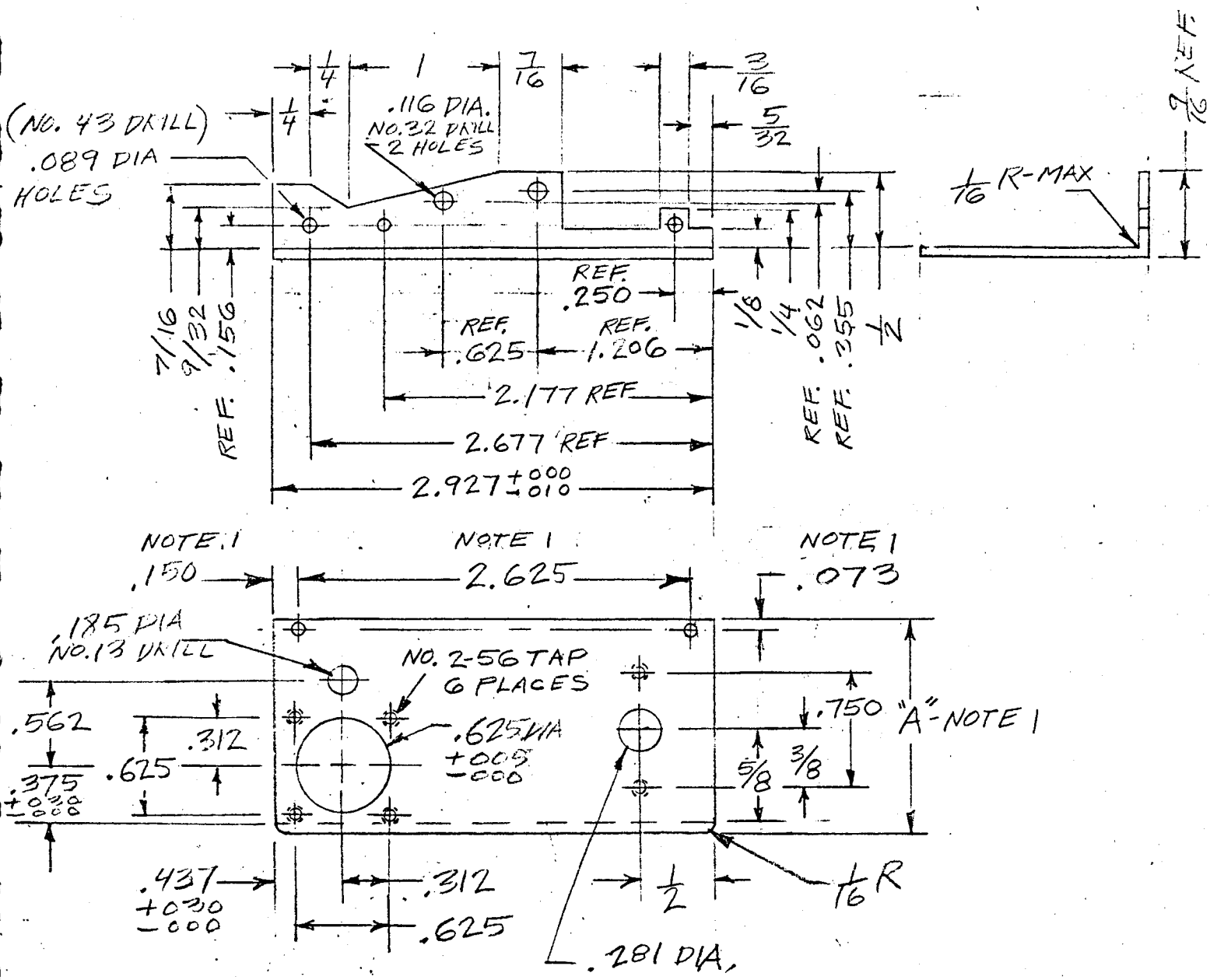
SCALE: FULL

MATL: 6 1/4 × 5 15/16 × .062 ± .002 ALUM. ALLOY 5052 H32

TOL.: +.020 -.000

LAYOUT - CASE, TRANSCEIVER (REFERENCE ONLY)

SKETCH 2-A

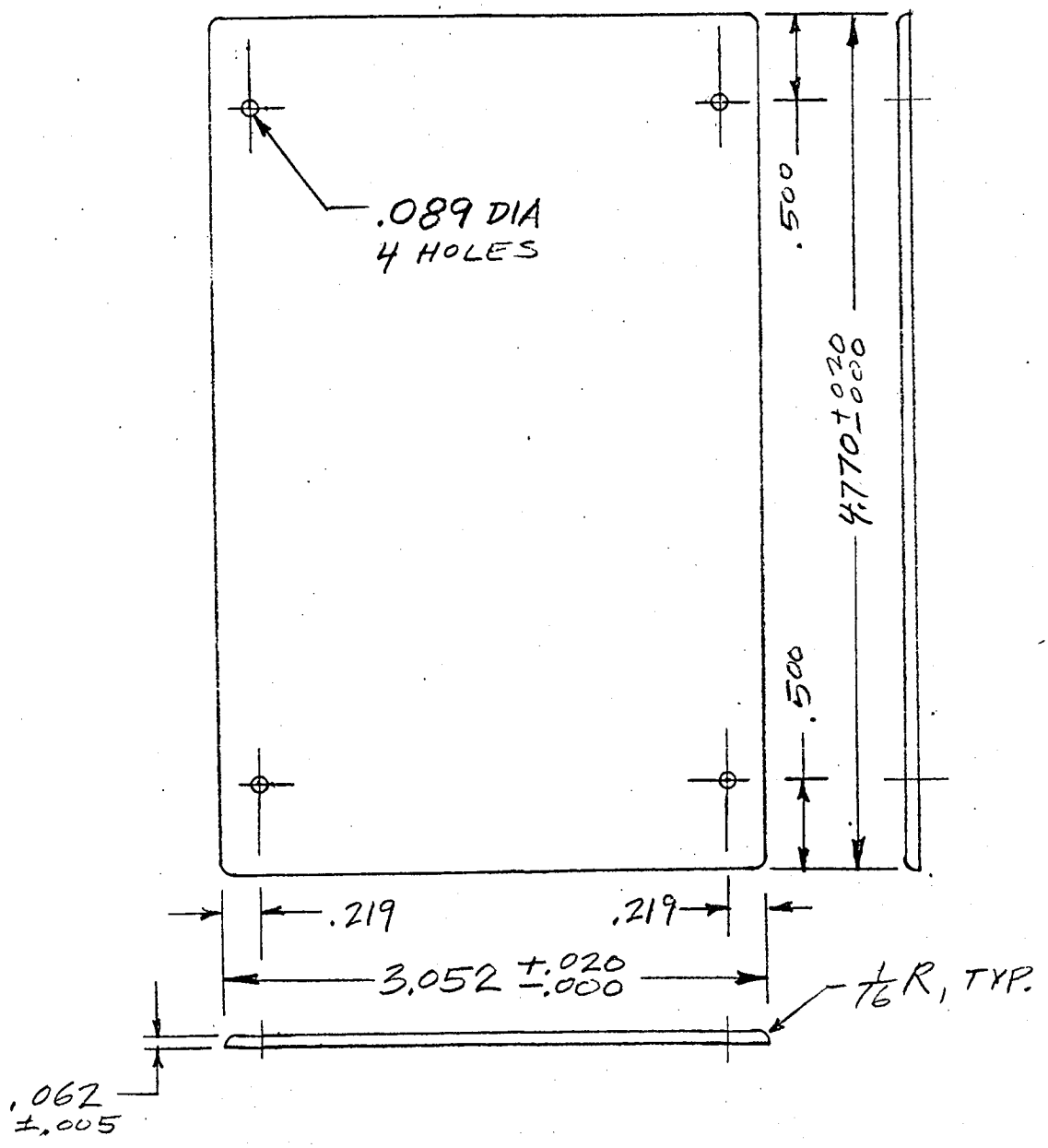


NOTES 1. DIM. "A" = 2 ± 1/16 INITIALLY. DURING ASSEMBLY, BRACKET SHALL BE SHEARED TO FIT. "A" WILL THEN BE APPROX. 1.475. THE TWO .089 DIA. HOLES IN THE LOWER VIEW SHALL BE DRILLED AFTER THE SHEARING OPERATION.

2. ALL HOLES IN THE UPPER VIEW SHALL BE LOCATED DURING ASSEMBLY BY LINE DRILLING THRU THE MATING HOLES IN THE MOTHER BOARD, SKETCH 5. (5 HOLES)

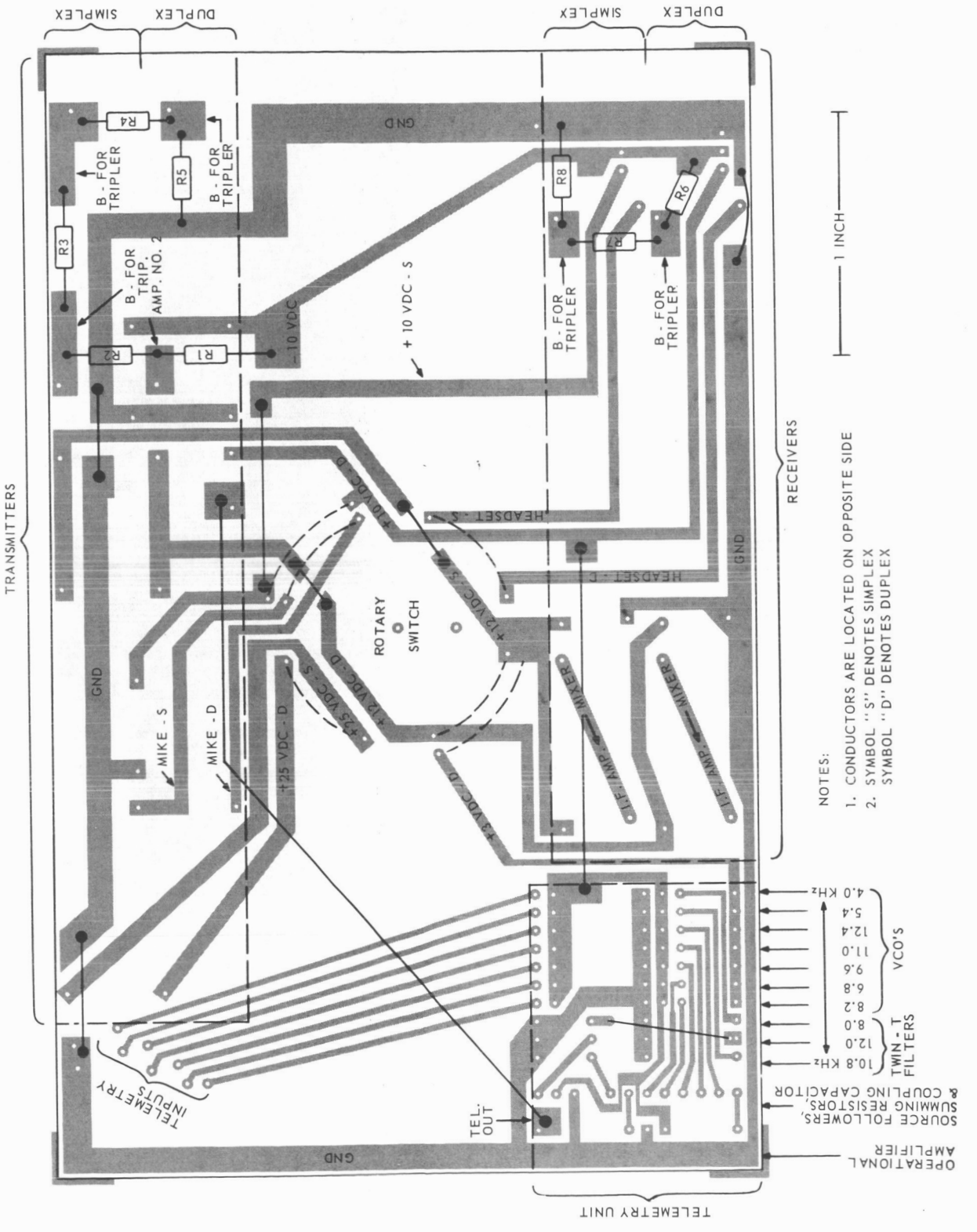
SCALE - FULL
TOL. - DEC, ± .005
FRAC. ± .015
MAT'L - ALUM. ALLOY 5052 H32
.062 ± .002 THK

SKETCH 3
BRACKET - TRANSCEIVER

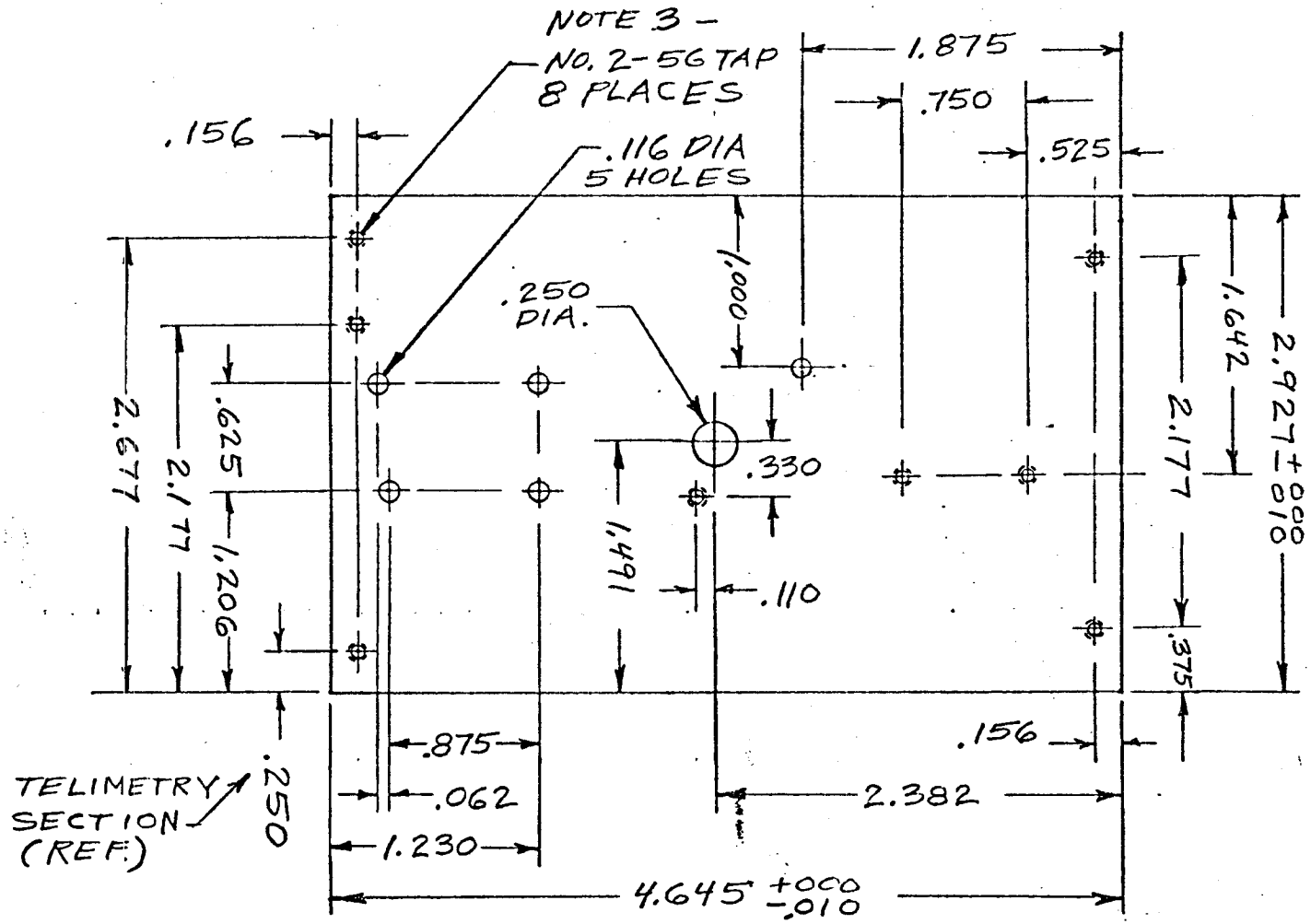


SCALE - FULL
MAT'L - ALUM. ALLOY 5052 H32
TOL ±.010

COVER - TRANSCEIVER
SKETCH 4



Sketch 5. Mother Board (Printed Circuit)



SCALE- FULL
TOL- ±.005
MAT'L - .062 ± .002
THK. FIBERGLASS,
2 OZ. SINGLE
CLAD COPPER.

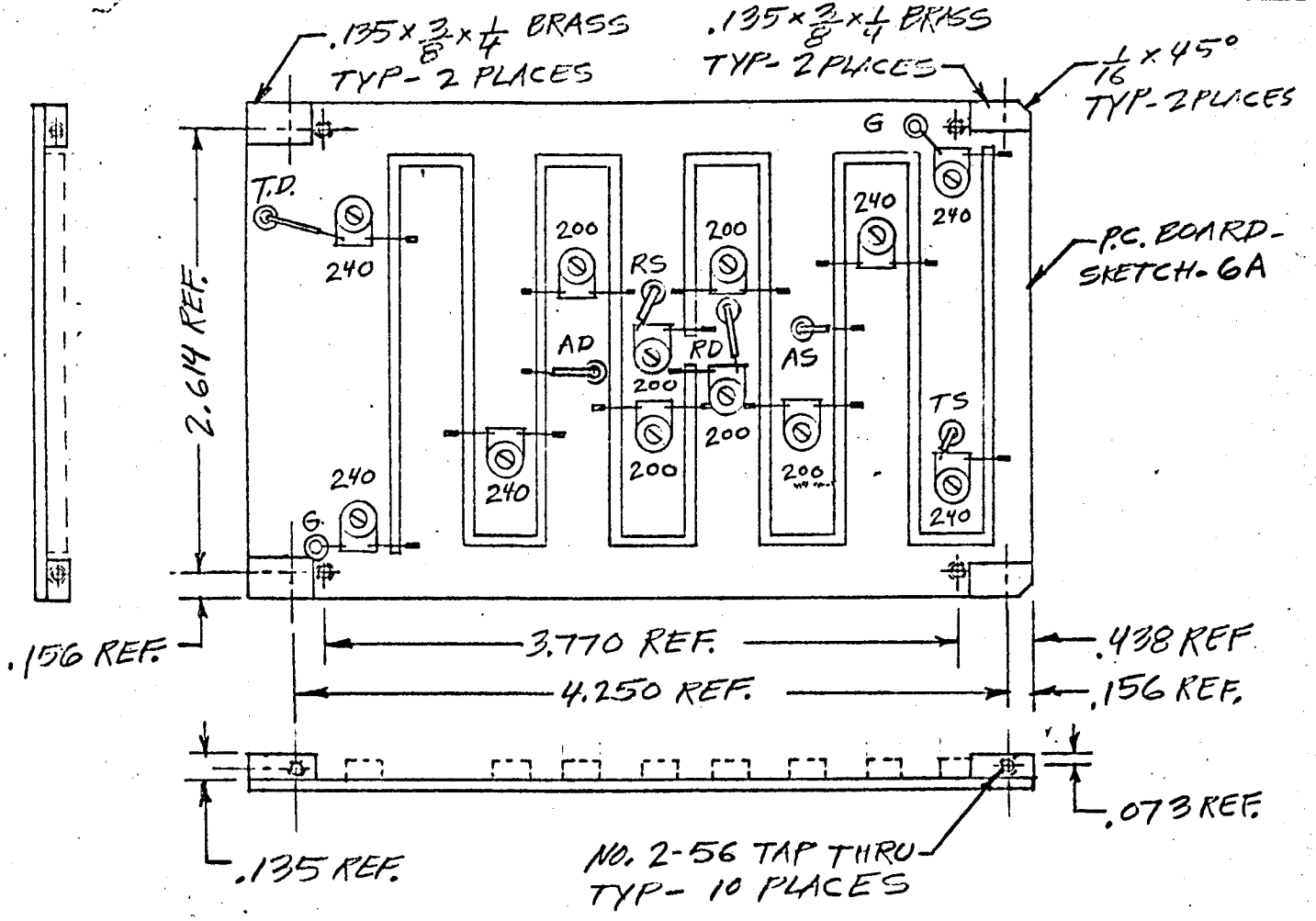
NOTES: 1. ALL DIMENSIONS ARE WITH RESPECT TO INBOARD EDGES OF PRINTED CORNER MARKS. ALL HOLES MUST BE LOCATED BEFORE TRIMMING BOARD TO FINAL SIZE, SINCE CORNER MARKS ARE CUT OFF IN THIS OPERATION.

2. CONDUCTORS ARE ON OPPOSITE SIDE.

3. DO NOT TAP UNTIL PILOT HOLES HAVE BEEN DRILLED IN CASE & BRACKET (SKETCHES 2 & 3) USING A NO. 50 TAP DRILL & THE MOTHER BOARD AS A DRILL JIG.

4. SMALL HOLES (.025 DIA.) ARE NOT SHOWN.

SKETCH 5
MOTHER BOARD
(SHEET 2 OF 2)



NOTES:

1. FASTEN THE 4 BRASS CORNER PIECES TO THE FIBERGLASS BOARD USING EPOXY CEMENT.
2. LOCATE THE 4 HOLES IN THE FIBERGLASS BOARD BY CENTERING AND CLAMPING THE BOARD ONTO THE COVER, SKETCH 4, AND THEN BY LINE DRILLING THE COVER HOLES USING A NO. 2-56 TAP DRILL.
3. LOCATE THE 6 HOLES IN THE BRASS PIECES DURING ASSEMBLY BY LINE DRILLING THRU THE MATING HOLES IN THE CASE AND BRACKET, SKETCHES 2 AND 3, RESPECTIVELY. (THE DIPLEXER SHOULD BE FASTENED TO THE COVER, SKETCH 4, DURING THIS OPERATION.)
4. SYMBOLS FOR TERMINALS
   - D - DUPLEX
   - S - SIMPLEX
   - A - ANTENNA
   - R - RECEIVER
   - T - TRANSMITTER
   - G - GROUND
5. CAPACITORS.
   - MT 200 = 4/15 pf - 6 REQ'D
   - MT 240 = 6.5/40 pf - 6 REQ'D

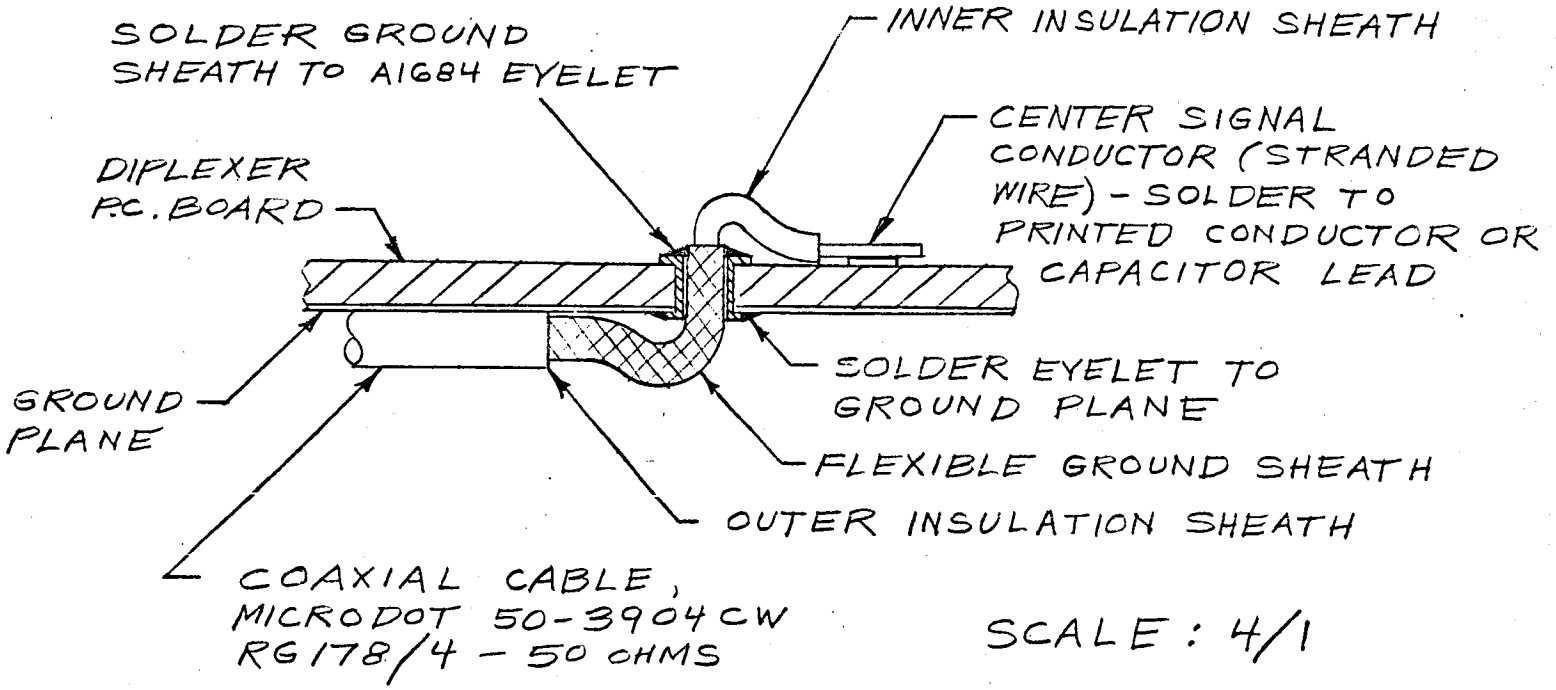
SCALE - FULL
TOL. - DEC. ±.005
FRACT. ±.015

DUAL DIPLEXER
SKETCH 6 (SHEET 1 OF 2)

6. SOLDER LEADS ON PRINTED CONDUCTORS AT LOCATIONS INDICATED BY PRINTED GUIDE MARKS.

7. WHERE A CAPACITOR LEAD IS CONNECTED TO A FLEXIBLE, STRANDED WIRE (TRANSMITTER AND RECEIVER TERMINALS), FASTEN THE CAPACITOR LEAD TO THE P.C. BOARD USING EPOXY CEMENT. THE SOLDERED, SOLID WIRE LEADS AT ALL OTHER POINTS ARE SUFFICIENTLY RIGID TO HOLD THE CAPACITOR IN A FIXED POSITION DURING CAPACITOR TUNING, SHOCK, OR VIBRATION.

8. CONNECT COAXIAL CABLES AS SHOWN BELOW: (6 PLACES)

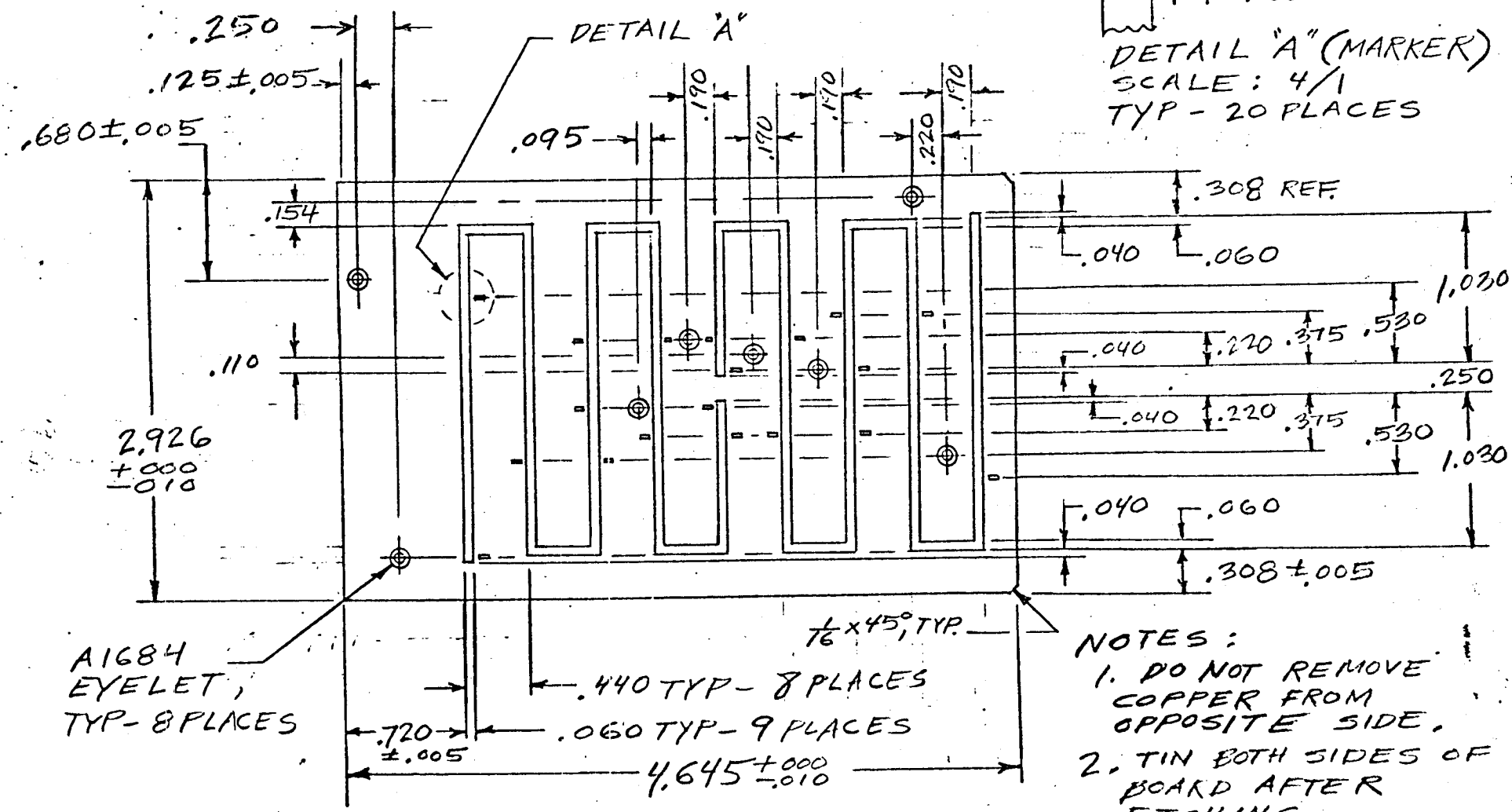


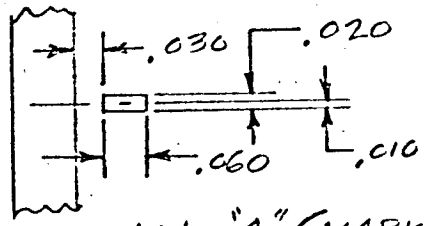
SCALE: 4/1

9. APPROXIMATE CABLE LENGTHS ARE LISTED BELOW:

AD	5 1/2	INCHES
RD	5 1/2	
TD	1 3/4	
AS	8	
RS	4 3/4	
TS	7	

DUAL DIPLEXER
SKETCH 6 (SHEET 2 OF 2)





DETAIL "A" (MARKER)
SCALE: 4/1
TYP - 20 PLACES

NOTES:
1. DO NOT REMOVE COPPER FROM OPPOSITE SIDE.
2. TIN BOTH SIDES OF BOARD AFTER ETCHING.

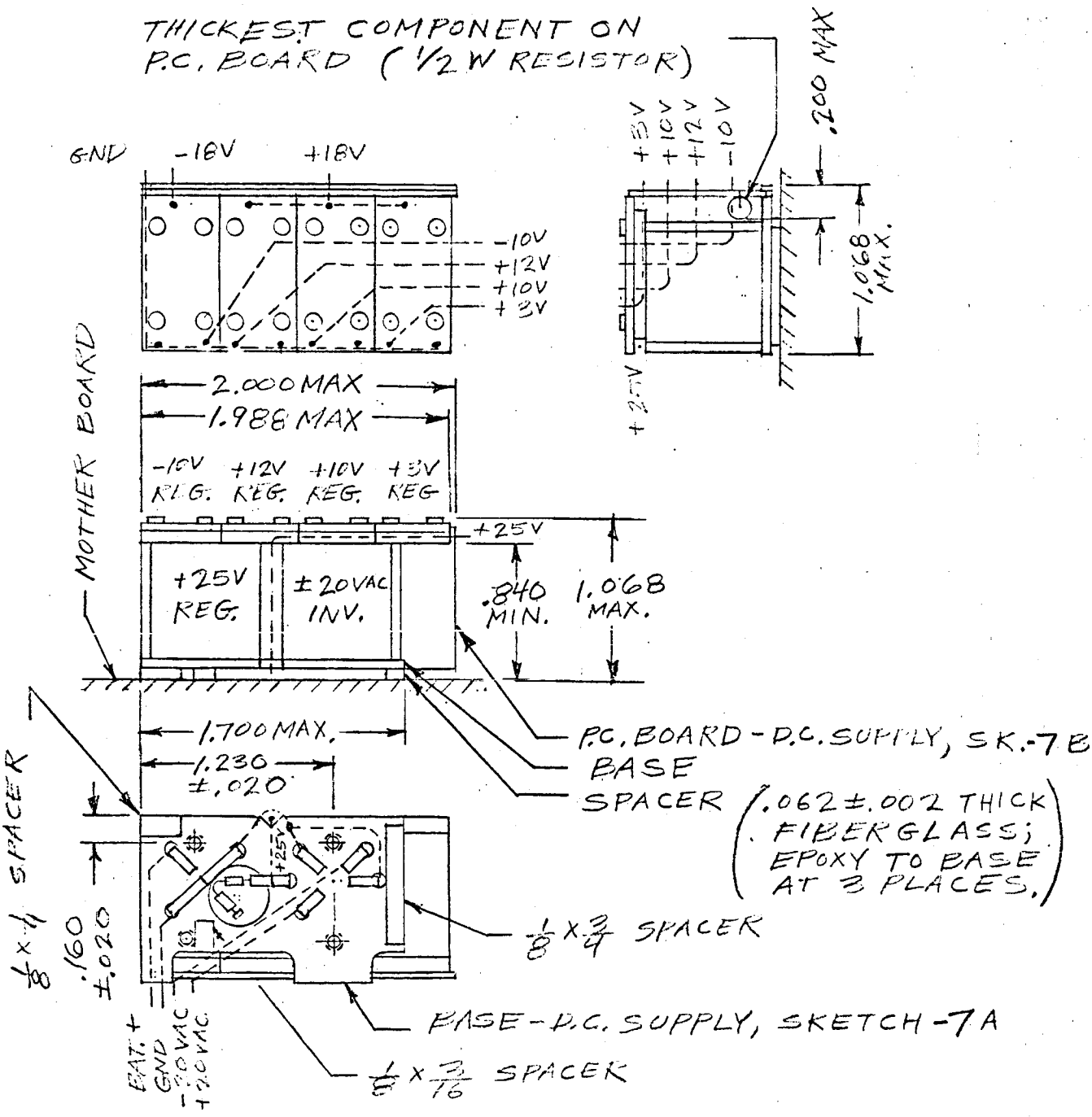
SCALE: FULL

MAT'L: .058±.001 THK. FIBERGLASS,
2 OZ. DOUBLE CLAD COPPER.
(.062 THK. INCLUDING COPPER.)
DIELECTRIC CONSTANT = 12.5 ± 1%.

TOL. UNLESS OTHERWISE SPECIFIED:
DEC. ±.002, FRACT. ±.015

P.C. BOARD -
DUAL DIPLEXER
SKETCH-6A

NOTE 4- REMOVE THOSE PORTIONS OF POWERCUBE MODULES CONTAINING MOUNTING HOLES, SUCH THAT THE 1.500" DIMENSION IS REDUCED TO .820 ± .030.



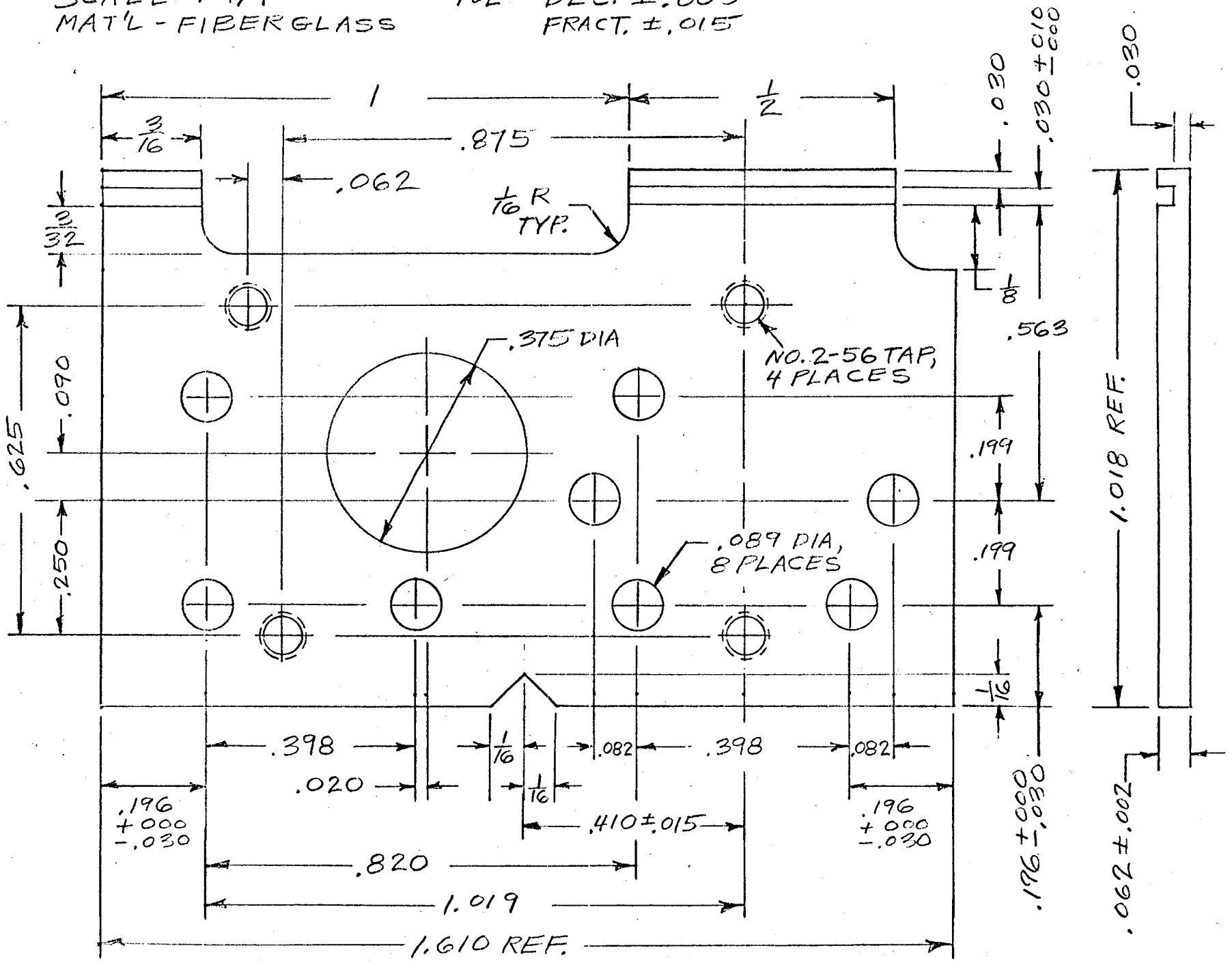
NOTES:
1. DOTTED LINES REPRESENT WIRES.
2. ALL DIMENSIONS ARE FOR REFERENCE ONLY, EXCEPT FOR SPACERS.
3. CEMENT HELIPOT REGULATORS TO POWERCUBE REGULATOR & INVERTER USING HEAT CONDUCTING EPOXY.

SCALE: FULL

SKETCH 7
D.C. POWER SUPPLY

SCALE : 4/1
MAT'L - FIBERGLASS

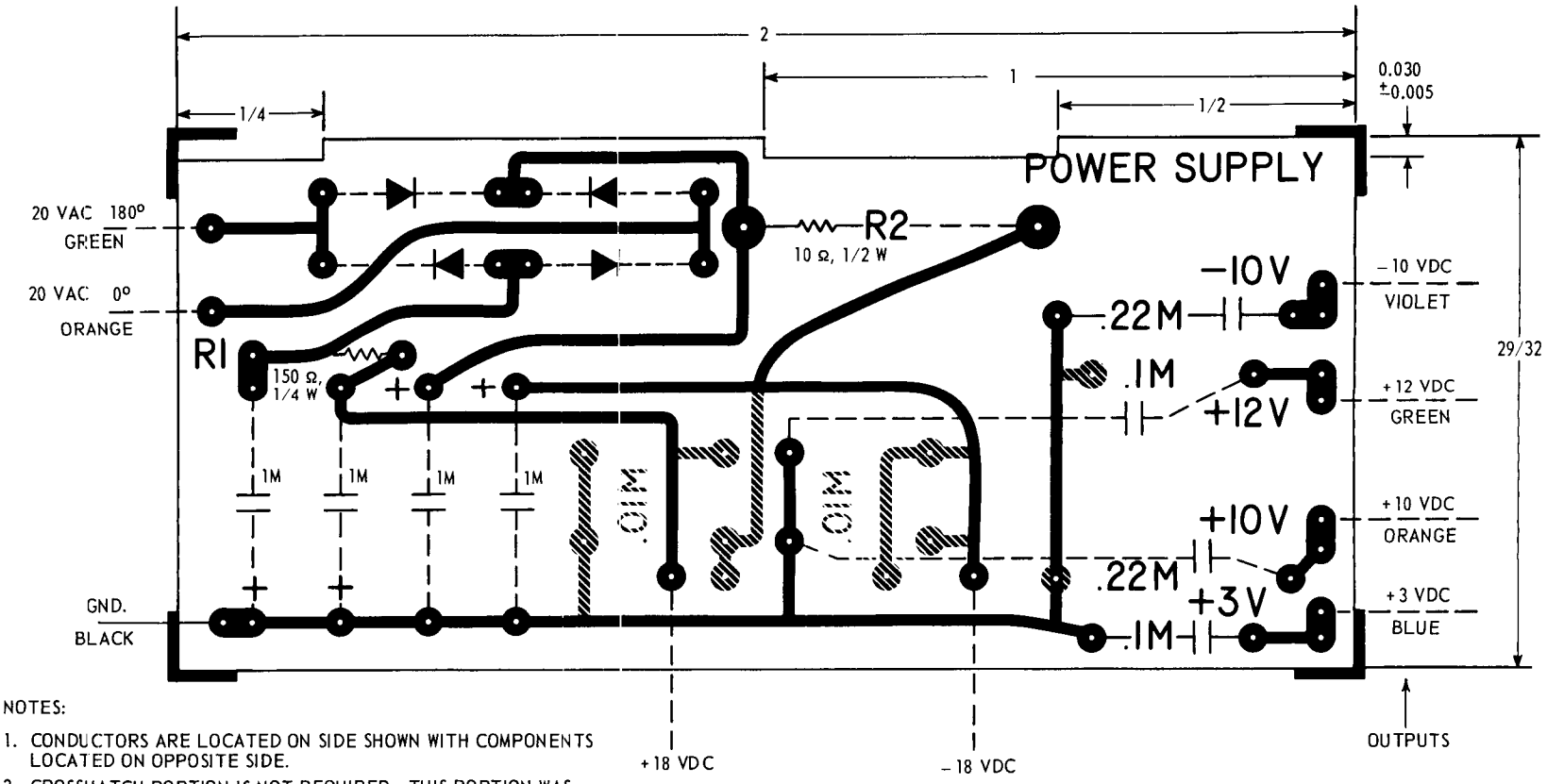
TOL - DEC. ±.005
FRACT. ±.015



SKETCH 7A

BASE - D.C. SUPPLY

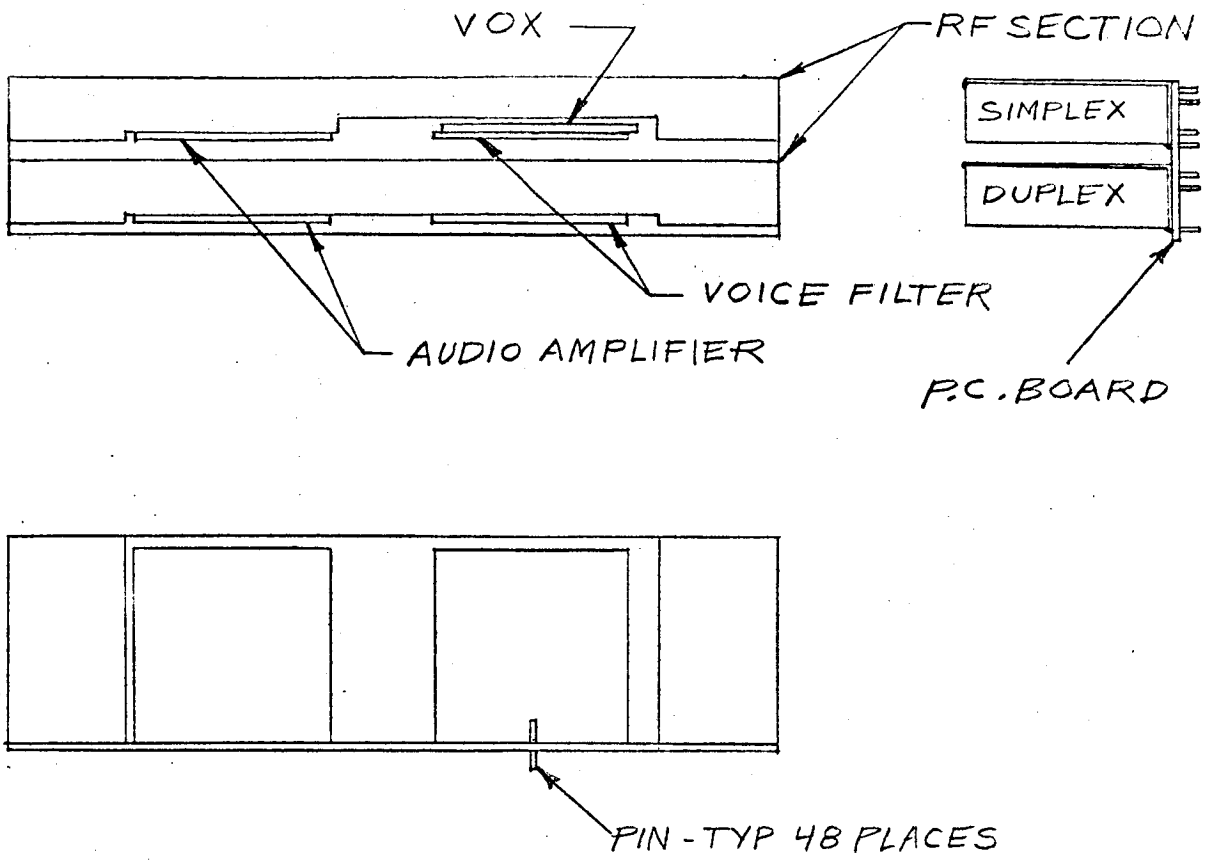
B0406



NOTES:

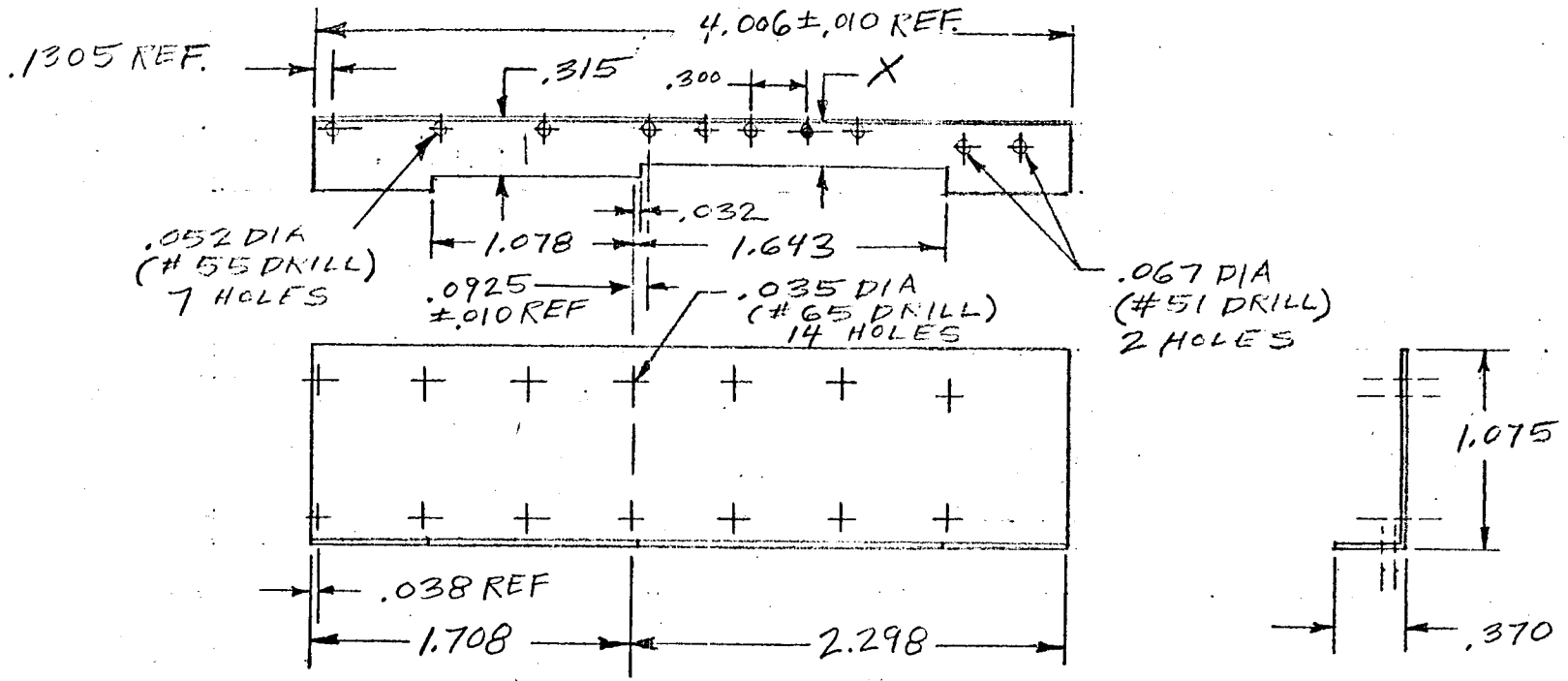
1. CONDUCTORS ARE LOCATED ON SIDE SHOWN WITH COMPONENTS LOCATED ON OPPOSITE SIDE.
2. CROSSHATCH PORTION IS NOT REQUIRED. THIS PORTION WAS INTENDED FOR CONNECTION OF A 0.01 μf CAPACITOR FROM THE INPUT TO GROUND TERMINALS OF EACH OF THE FOUR OUTPUT VOLTAGE REGULATORS (HELIPOT). THIS WAS FOUND UNNECESSARY DUE TO THE SHORT DISTANCE FROM THE 1 μf CAPACITORS TO THE ABOVE REGULATORS. ELIMINATION OF THE 0.01 μf CAPACITORS, PERMITS LOCATION OF THE OUTPUT CAPACITORS (0.10 AND 0.22 μf) SO THEY DO NOT OVERLAY ONE ANOTHER AND THUS REDUCES THE THICKNESS OF THE ASSEMBLED P.C. BOARD.
3. TOL., UNLESS OTHERWISE SPECIFIED, ±0.015
4. MAT'L. 0.030 THK, FIBERGLASS, 2 OZ. SINGLE CLAD COPPER
5. TIN CONDUCTORS AFTER ETCHING
6. DRILL 0.022/0.025 DIA. HOLES

Sketch 7B. PC Board - DC Power Supply



SCALE-FULL

SKETCH 8
DUAL TRANSMTTER

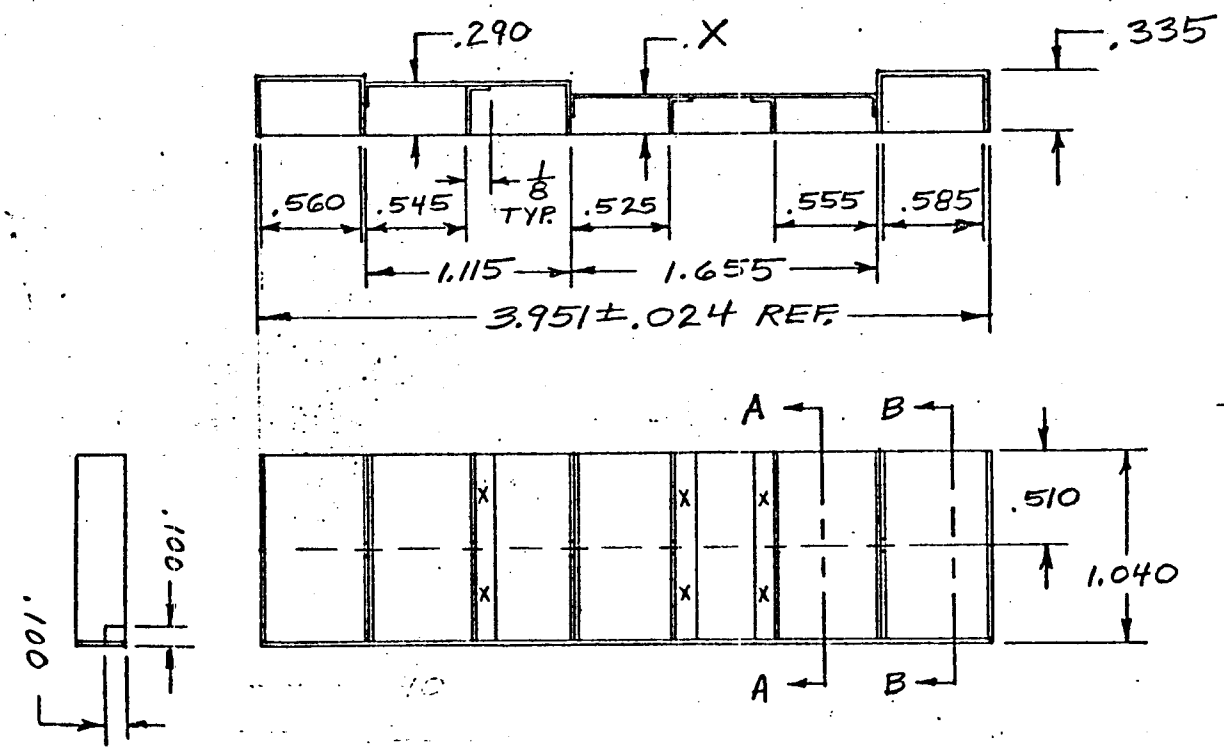


NOTE

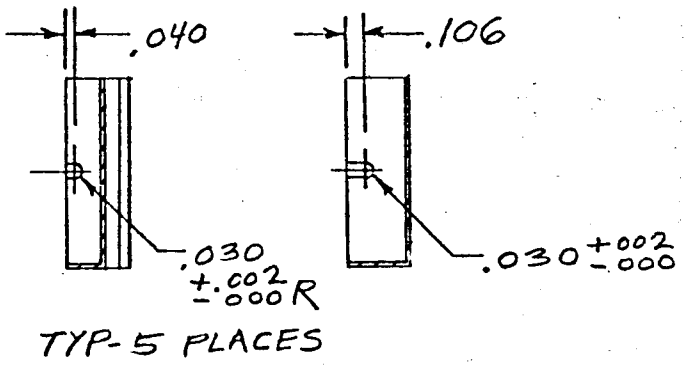
X = .250 FOR SKETCH 8A (SIMPLEX)
X = .315 FOR SKETCH 8B (DUPLEX)

SCALE: FULL
TOL: ±.010, EXCEPT
HOLE DIA = $^{+.002}_{-.000}$
MATL - .008/.010 THK. BRASS
NOTE - LOCATE ALL HOLES USING DRILL JIG T-1

SKETCHES 8A AND 8B
BASE - TRANSMITTER
(RF PORTION)



SCALE - FULL
TOL. ±.005
±1/64
MAT'L. .008/.010 THK.
BRASS



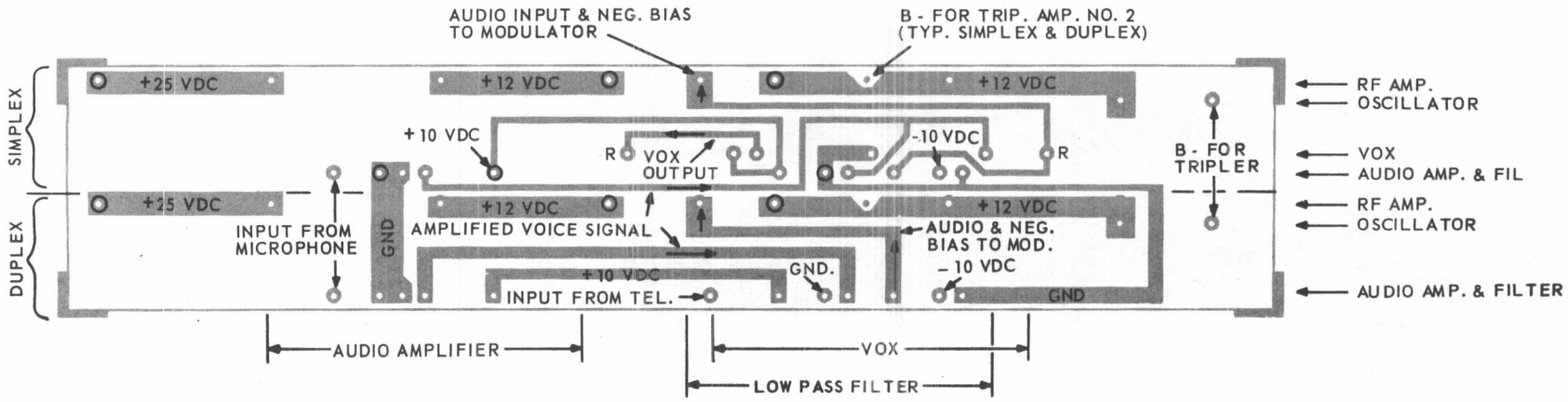
SECTION A-A

SECTION B-B

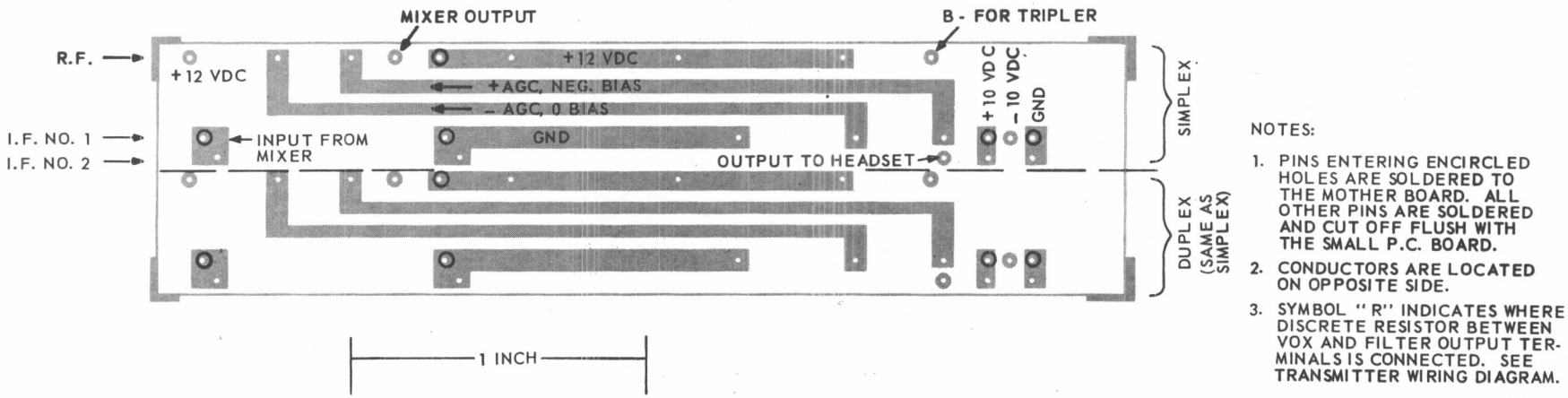
NOTE

X = .225 FOR SKETCH 8C (SIMPLEX)
X = .290 FOR SKETCH 8D (DUPLEX)

SKETCHES 8C AND 8D
COVER - TRANSMITTER
(RF PORTION)



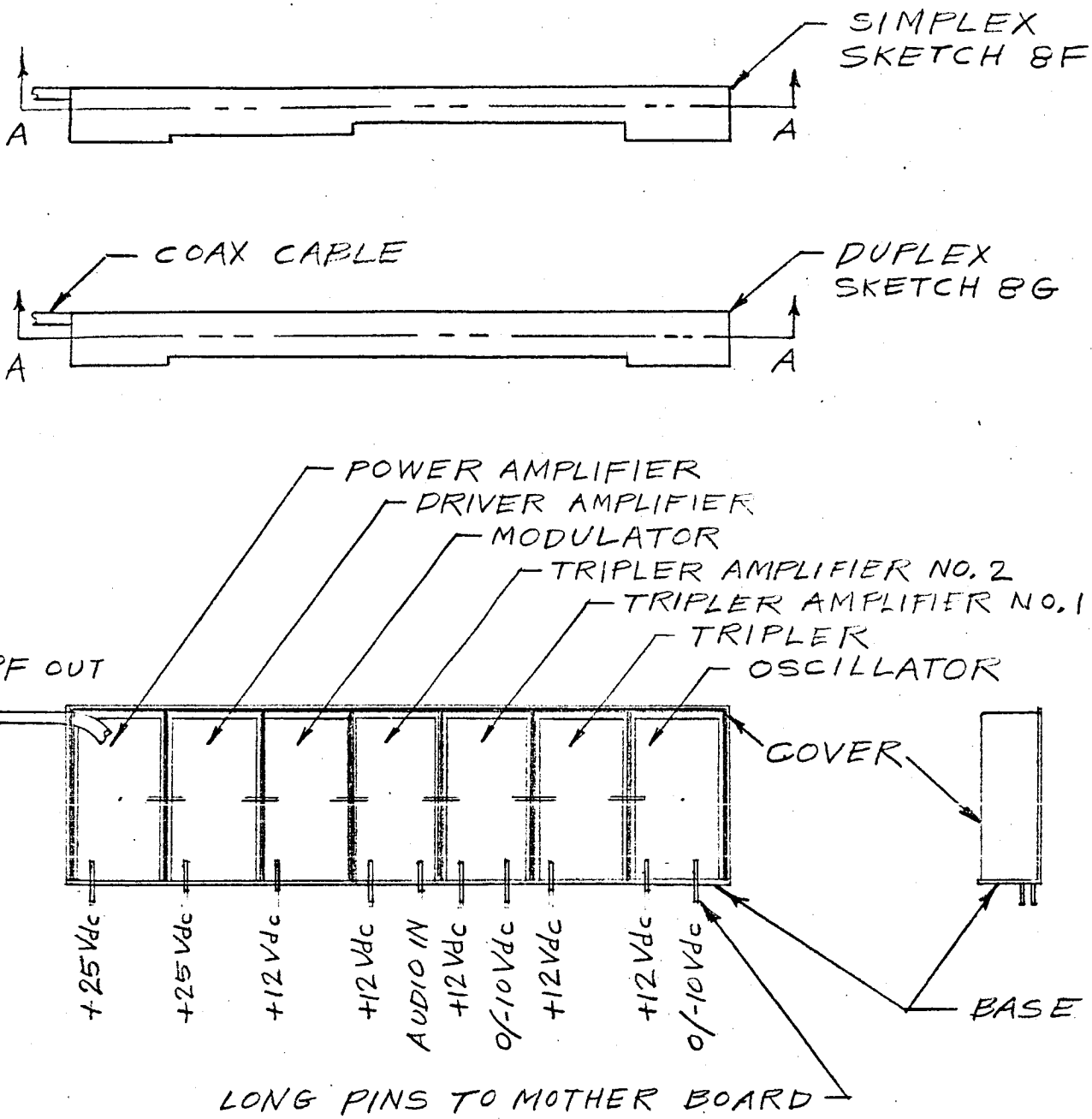
Sketch 8E. PC Board - Dual Transmitter



NOTES:

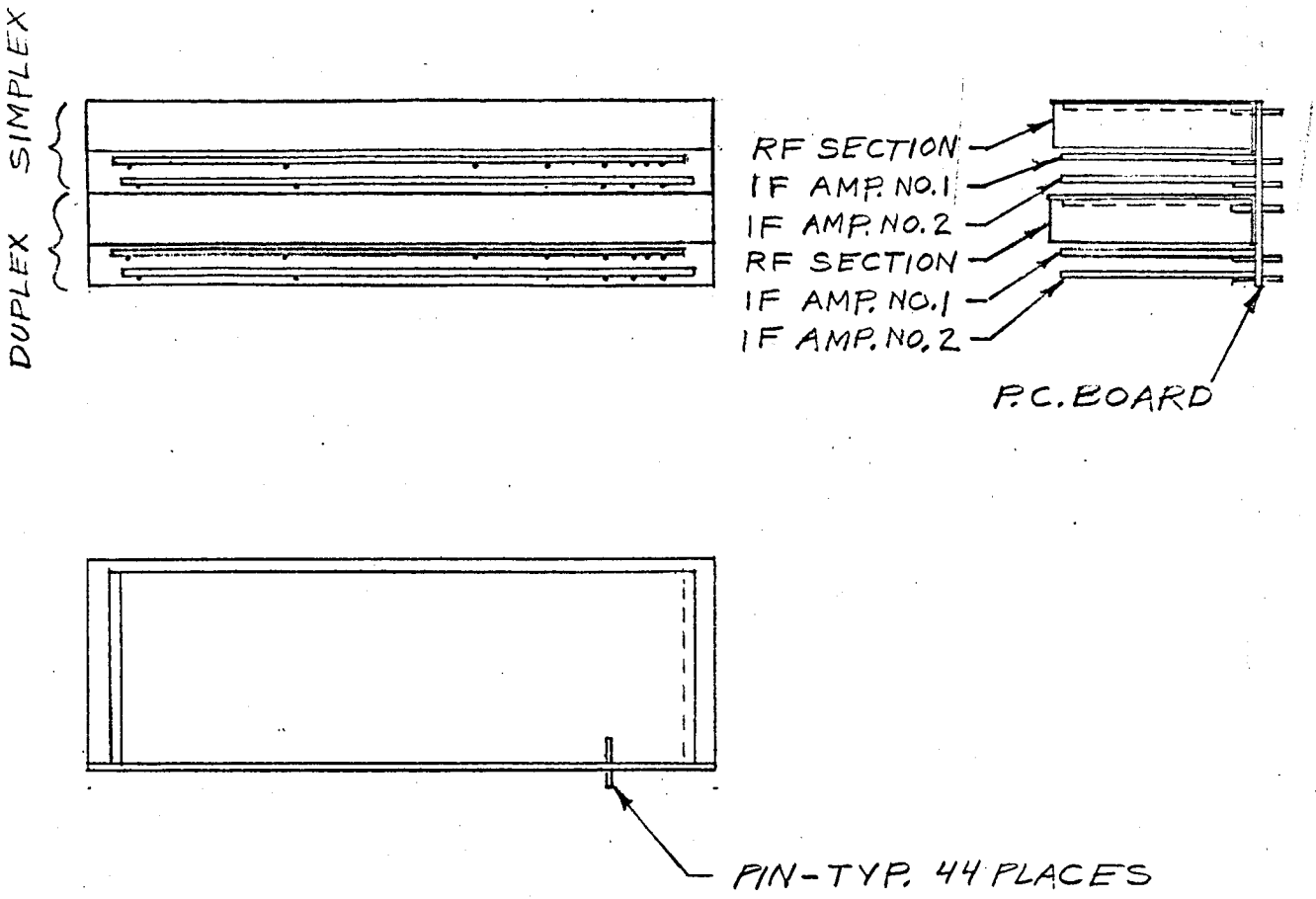
1. PINS ENTERING ENCIRCLED HOLES ARE SOLDERED TO THE MOTHER BOARD. ALL OTHER PINS ARE SOLDERED AND CUT OFF FLUSH WITH THE SMALL P.C. BOARD.
2. CONDUCTORS ARE LOCATED ON OPPOSITE SIDE.
3. SYMBOL "R" INDICATES WHERE DISCRETE RESISTOR BETWEEN VOX AND FILTER OUTPUT TERMINALS IS CONNECTED. SEE TRANSMITTER WIRING DIAGRAM.

Sketch 9C. PC Board - Dual Receiver



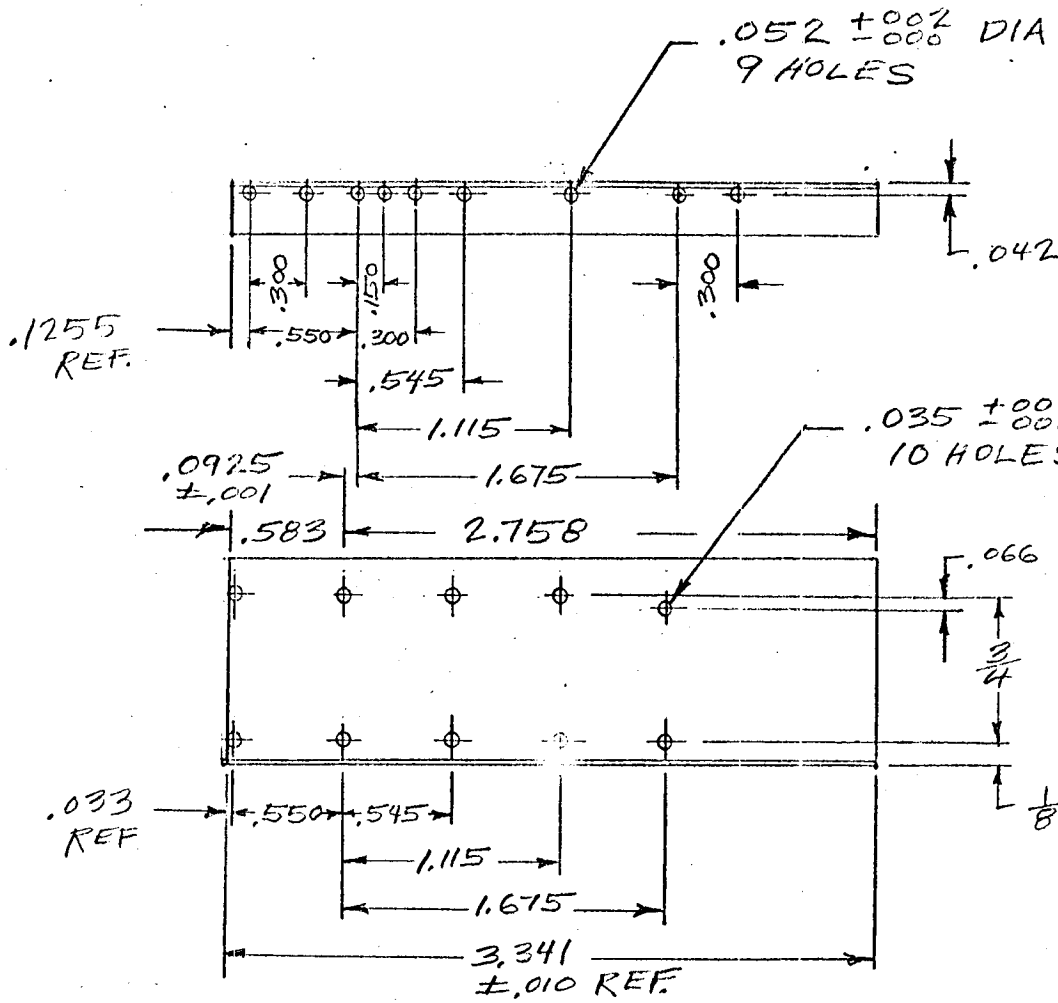
SECTION A-A

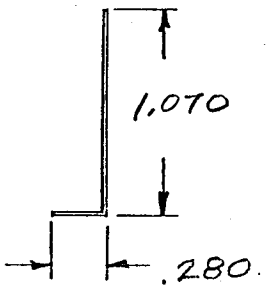
SKETCHES 8F AND 8G
RF SECTION -
TRANSMITTER



SCALE-FULL

SKETCH 9
DUAL RECEIVER



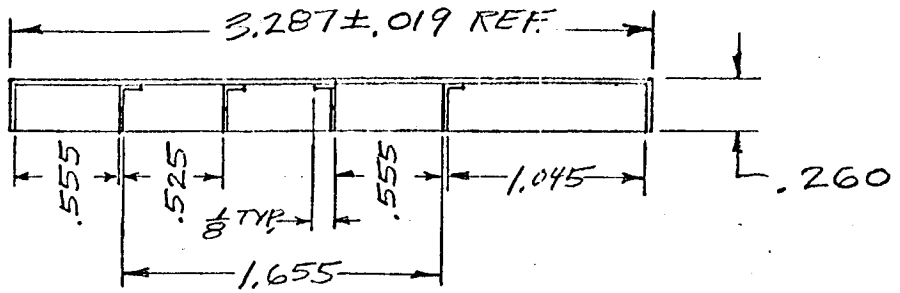


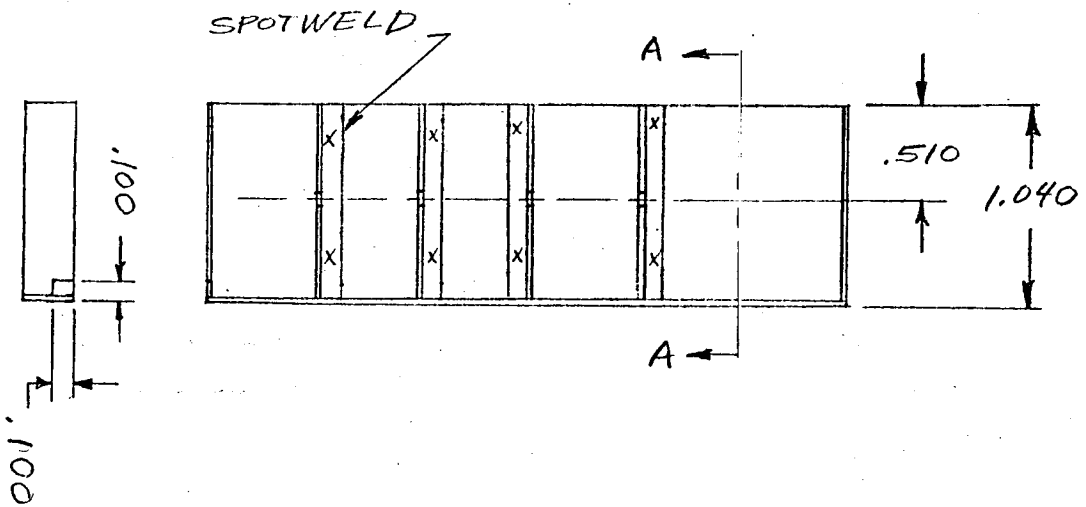
SCALE : FULL
TOL. ±.005
±1/32
MAT'L : .008/.010 THK. BRASS
NOTE - LOCATE HOLES USING DRILL JIG, SKETCH T-1

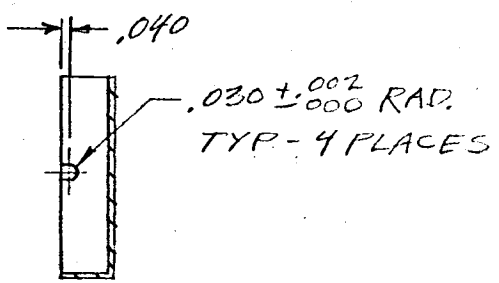
SKETCH - 9A

BASE - RECEIVER
(R.F. PORTION)

SCALE - FULL
TOL ±.005
±1/64
MAT'L: .008/.010 THK. BRASS

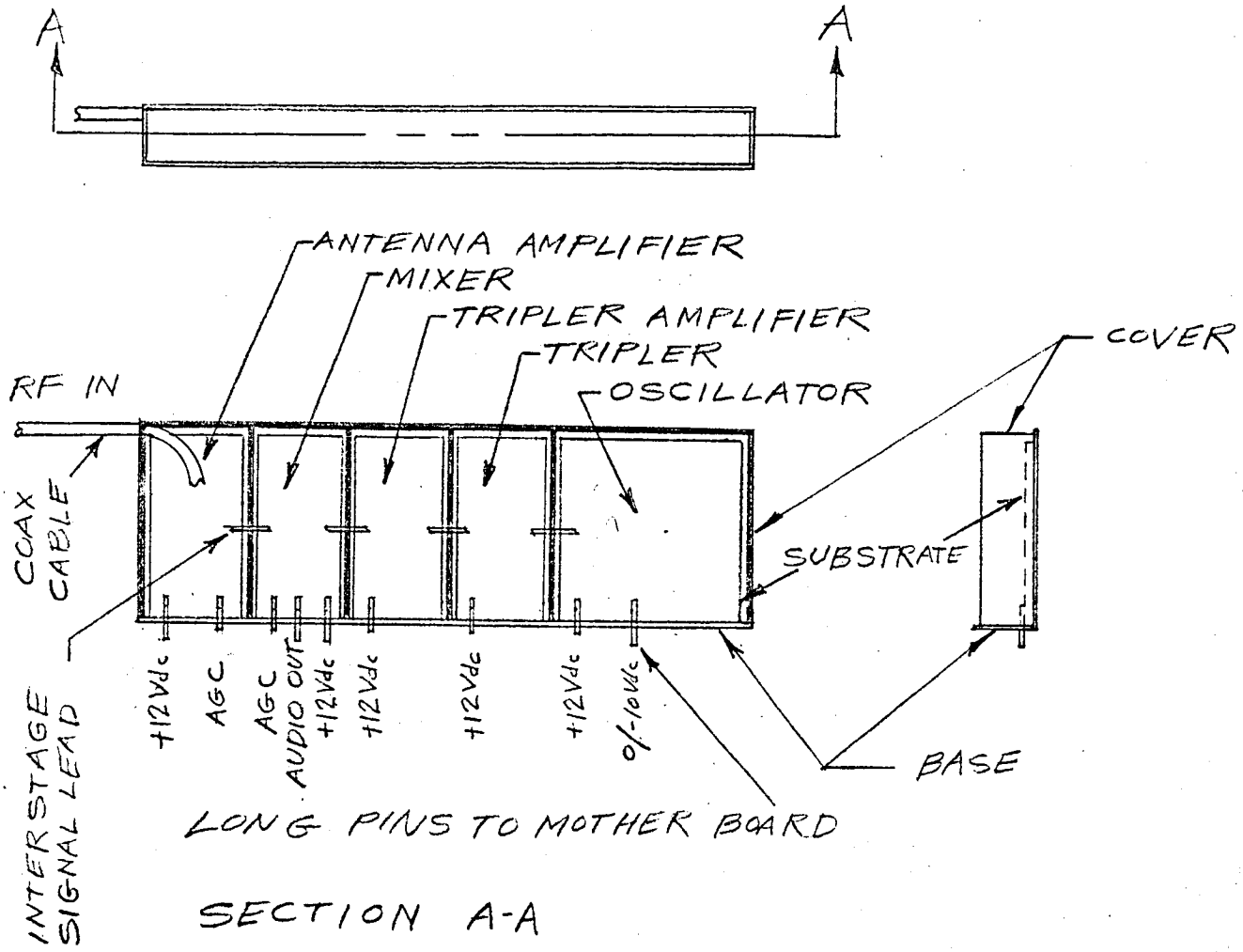






SECTION A-A

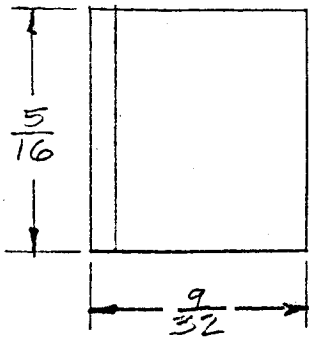
SKETCH-9B
COVER - RECEIVER
(RF PORTION)

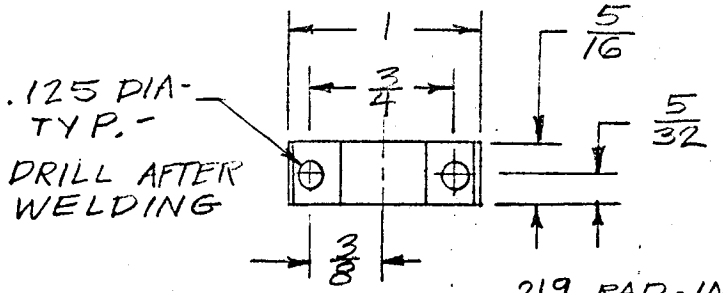


SECTION A-A

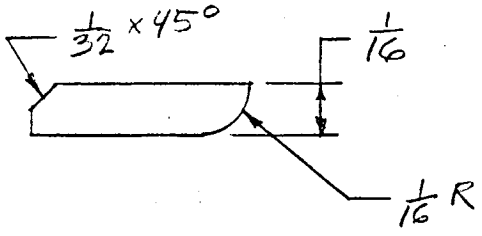
SCALE- FULL

SKETCH - 9D
RF SECTION - RECEIVER

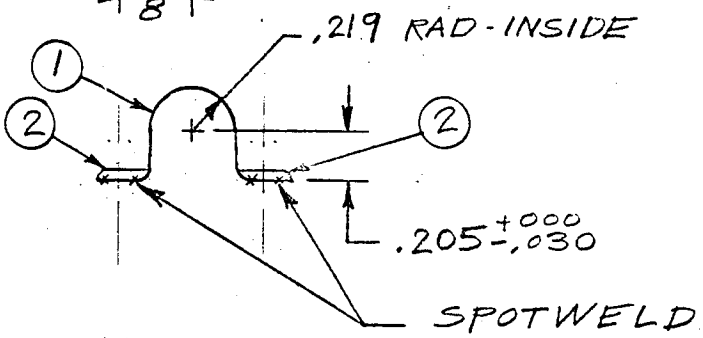




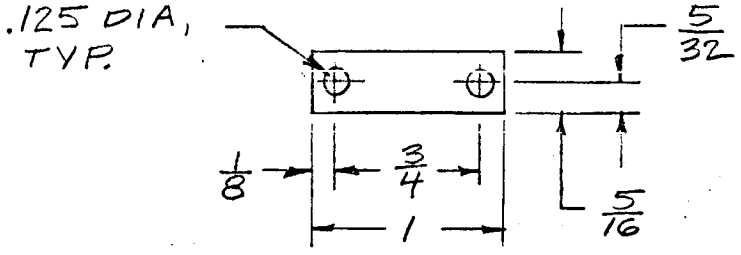
ITEM 1
MAT'L - .010 ± .001
THK. CRES
NO. 304



ITEM 2
SCALE - 4/1
MAT'L - CRES
NO. 304
2 REQ'D



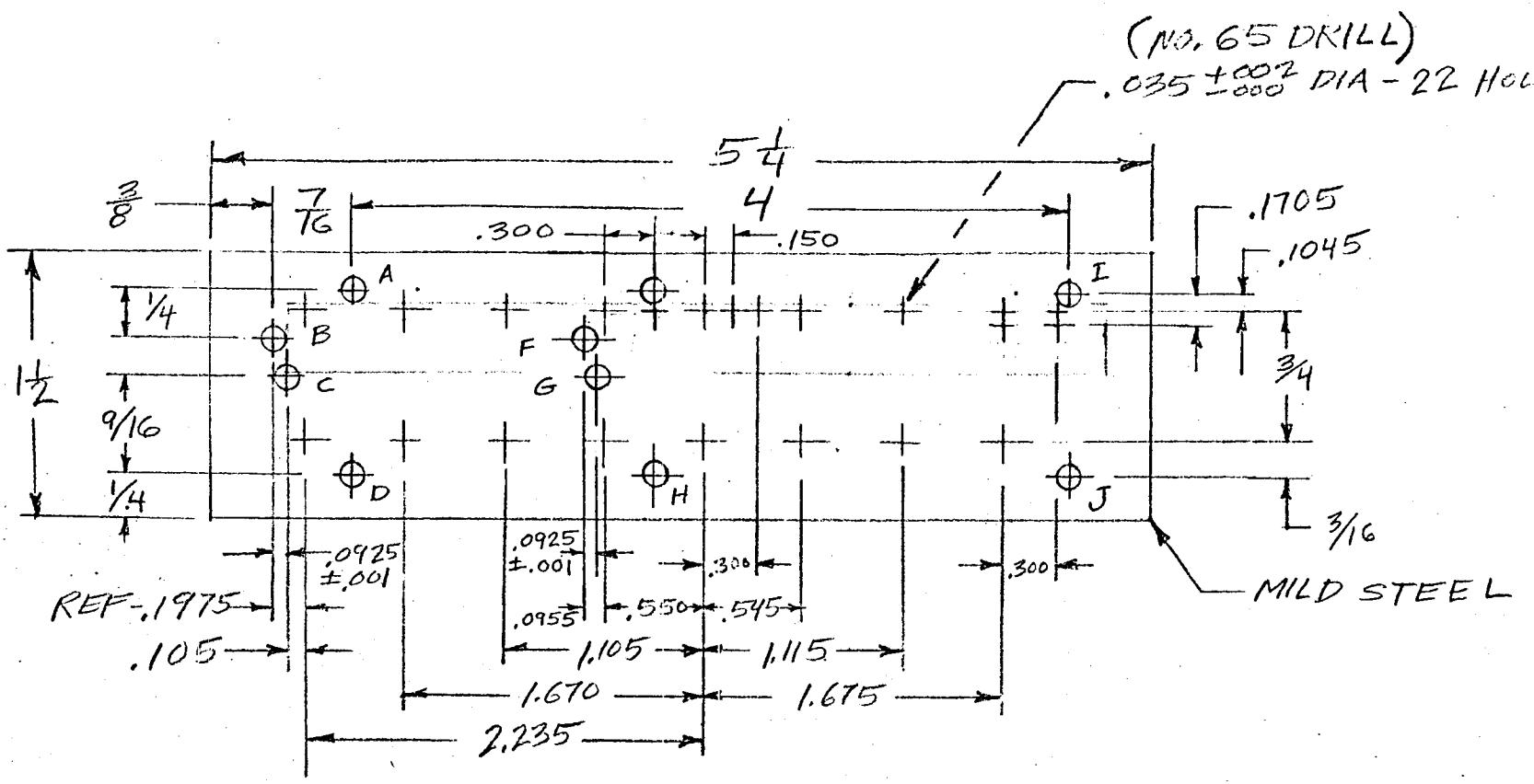
SCALE - FULL
SKETCH 10 A
CLAMP - COAX RELAY

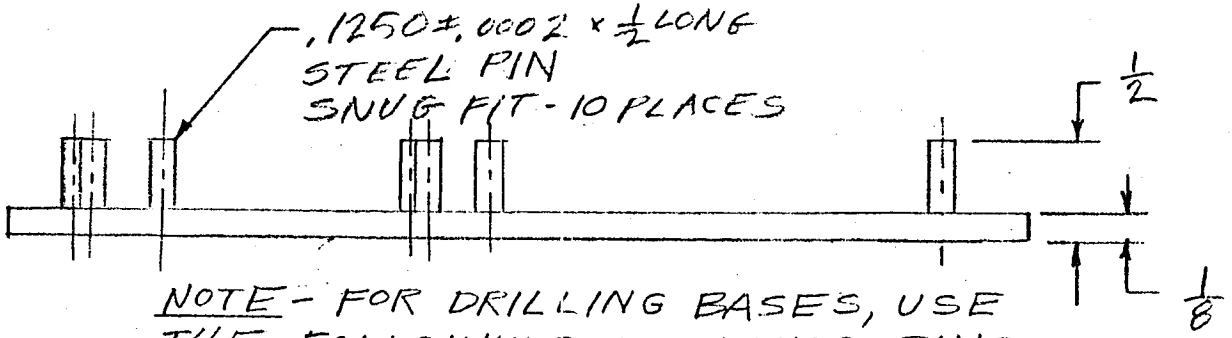


MAT'L -
.010 ± .001 THK
CRES NO. 304

SCALE - FULL
SKETCH 10 B
SHIM - COAX RELAY

TOL - FRACT. ± .015
DEC. ± .005





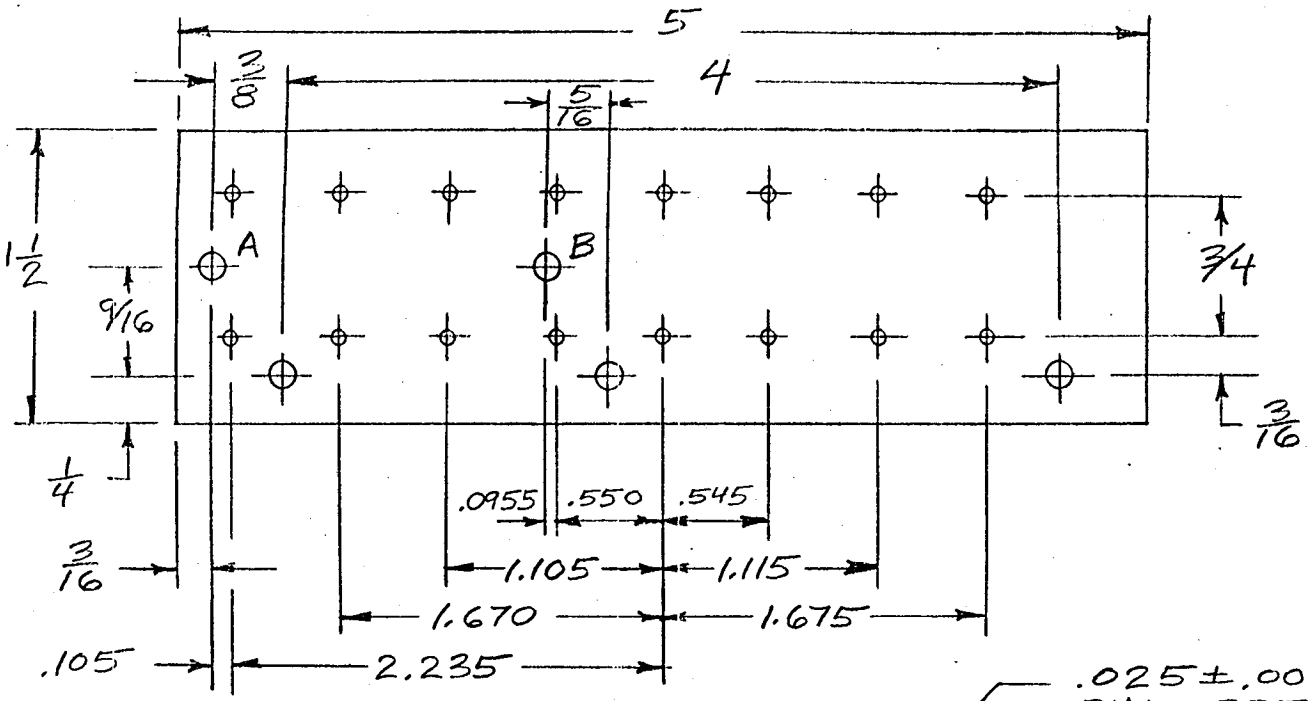
NOTE - FOR DRILLING BASES, USE THE FOLLOWING LOCATING PINS; REMOVE ALL OTHER PINS:

TRANSMITTER - WIDE PORTION - C D J
NARROW - B A I

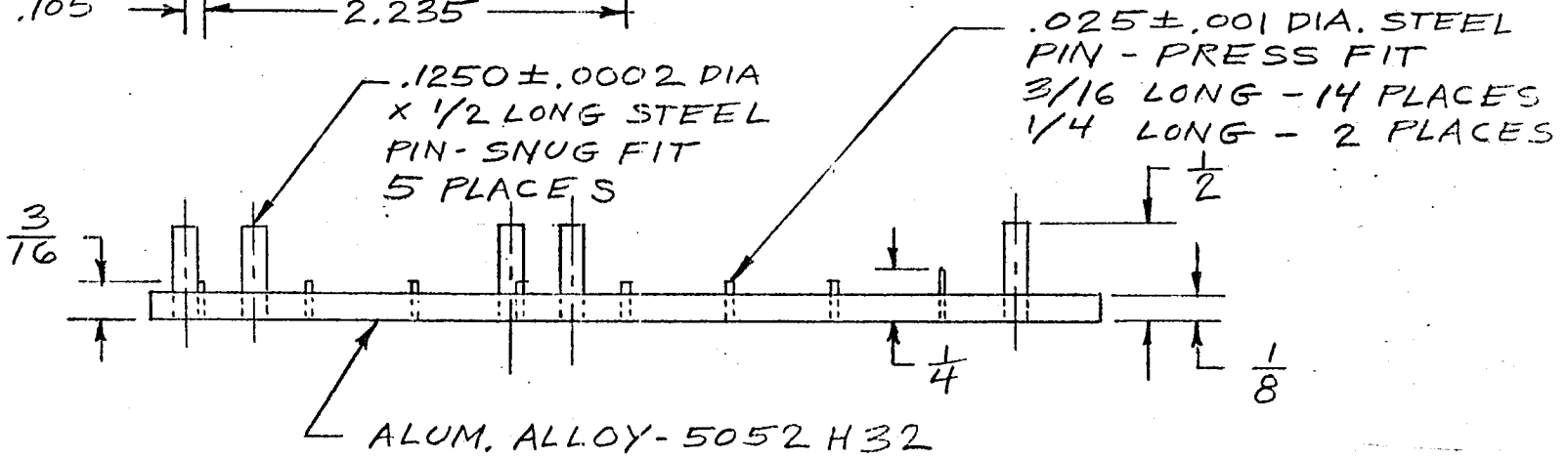
RECEIVER - WIDE - G H J
NARROW - F E I

SCALE: FULL
TOL: ± .005
± 1/64

SKETCH T1
DRILL JIG - BASE



SCALE - FULL
TOL - DEC ±.005
FRACT. ±.015



NOTES 1. LOCATE ALL HOLES USING DRILL JIG, SKETCH T-1

2. USE PIN A FOR TRANSMITTERS;
USE PIN B FOR RECEIVERS

SKETCH T-2

LOCATING JIG -
SUBSTRATE TO BASE

APPENDIX A-1

Thin Film Circuit Processing

The thin film circuits for this program were vacuum deposited, using aperture masks. Substrate batch area was 4" x 4". All evaporant sources were located about 21" below the center of the substrate batch. A shutter, located about 1 inch below the substrate batch, was used to block the vapor stream during outgassing. All substrates were .021 ±.003" thick, Corning Code 0211 glass. Batches consisted of sixteen 1" x 1" substrates for all circuits, except the I.F. amplifiers where batches consisted of four 1" x 4" substrates. For the I.F. amplifiers, the ends of the substrate were scribed and broken off after deposition, such that the final size was 1" x 3". For the Universal RF substrates, two circuits were deposited per substrate. The RF substrates were cut in half after deposition to yield two 1" x 0.5" circuits per substrate.

All sources were heated by electron bombardment from a 1.3 inch diameter ring cathode. Positive D.C. voltage was applied to the source with the cathode at D.C. ground. The tungsten cathode (filament) was resistance heated sufficiently to emit electrons by 17 ± 1 amps at 10.4 ± 1 volts rms at 60 Hz.

All source materials were placed in crucibles which were election bombarded, except Re, which was bombarded directly.

All crucibles had outside dimensions of 0.50 inch diameter x 1.75 inch long. All crucibles had a depth of 1.53 inches. Crucible I.D. was .42" for all meterials except Al and Cu where the inside diameter was .38". Crucible material was Mo for all source materials except Al where an intermetallic composite of 50% BN + 50% TiB_2 was used. The Re souce slug, which was mounted on top of a .070" diameter Re rod, had a diameter of 0.375" and a length of 0.72" to 0.16"

All masks were fabricated by photo-etching of 3 mil thick Mo foil. Masks and substrates were retained in Mo pallets resembling window frames. Mask to substrate clearance was 5 mils for all circuits, except for RF circuits, where the substrates and masks were in contact, and during Re resistor depositions, where the clearance was 60 mils.

All deposition processes necessary for the complete fabrication of a batch of thin film circuits were performed during one continuous evacuation of the vacuum chamber. At times, more than one batch of substrates were fabricated during a single pumpdown. This was made possible by remotely controlled positioners for changing and registering masks and substrates, for changing sources, and for opening and closing the shutter.

Substrates were outgassed at 580 ± 10°C for 5 to 6 minutes. Sources were outgassed for 5 to 6 minutes each at a D.C. power 50 ± 5 watts below their maximum specified deposition power levels. All outgassing was performed at a vacuum of 10^{-4} torr or better.

Table 1 lists the names and part numbers of the ten circuits required for the system. The circuit part number is etched on the masks required for deposition of the circuit.

Table 3 is a general process chart which specifies the fabrication processes for all circuits, except the 5006-14 Universal RF Circuit, which is covered by Table 4. A separate chart is used for the RF circuit because of its dissimilarity with the other circuits. Table 2 contains data which is uniquely applicable to each circuit and which may be "plugged into" the blank spaces in Table 3 when depositing a particular circuit.

In the process charts, Tables 3 and 4, operations and the necessary steady-state conditions required during each operation are listed in chronological order. Limits or tolerances are specified for the directly controlled parameters. Values listed without tolerances are for reference information. Film thickness and rate of increase in film thickness are measured with a quartz crystal, film thickness monitor and differentiator (Sloan Model OMNI-II) in which thickness and thickness rate are displayed by frequency and frequency rate indicators. All other instrumentation is in common use.

For VCO and Twin-T-Filter circuits, the temperature coefficient of RC products must be between -150 and +200 PPM/°C. This requirement is met by the following specifications: $-70 \leq TCR \leq -170$ PPM/°C and $+20 \leq TCC \leq +270$ PPM/°C. For other circuits, the temperature coefficients may be 3 times the above values.

Capacitor working voltage is ±10 VDC for all circuits except RF circuits. For RF circuits, the working voltage is ± 12 VDC except for the driver and power amplifiers, for which the working voltage is ± 25 VDC.

Capacitor dissipation factor must be less than 1% at 1 KHz. Capacitor resistance must be greater than 1000 M ohms at 1.5 VDC. Operating temperature range is 0 to +50°C.

TABLE 1

THIN FILM CIRCUITS

PART NUMBER	NAME
R65018-1	Double Twin T Filter
5006-8	Voltage Controlled Oscillator (VCO)
5006-9	Source Followers, Summing Resistors and Coupling Capacitor
5006-10	Operational Amplifier
5006-11	Audio Amplifier - Transmitter
5006-12	Low Pass Filter and Bias for Transmitter Modulator
5006-13	I.F. Amplifier No. 1
5006-14	Universal R.F. Amplifier
5006-15	I.F. Amplifier No. 2
5006-16	Voice Operated Switch (VOX)

TABLE 2

CIRCUIT PROCESSING INFORMATION

				CIRCUIT DASH NO.									
				1	8	9	10	11	12	13	14	15	16
MASK DASH NO.	A	TERMINALS		6	7	1A	1A	1A	1A	1	7	1	1
	B	LOW VALUE RESISTORS		2	3	2	3	3	3	3	2	2	–
	C	HIGH VALUE RESISTORS		–	–	–	4	4	–	4	3	3	2
	D	LOWER CAPACITOR PLATES & CONDUCTORS		1	1	3	2	2	2	2	5	4	3
	E	CAPACITOR DIELECTRIC		3	4	4	5	5	4	5	4	6	4
	F	UPPER CAPACITOR PLATES & CONDUCTORS		4	5	5	6	6	5	6	1	5	5
	G	RESISTOR PROTECTIVE COAT		5A	6A	6A	7A	7A	6A	7A	6A	7	6
CAPACITOR DIELECTRIC		C/A DESIGN	PF/IN^2	64,500	→							65,500	→
		C/A ACTUAL	↓	61,275	61,200	59,400	64,500	→		87,800	50,000	55,600	62,000
		M ± 1%	GM.	1.348	1.350	1.390	1.280	→		0.940	1.650	1.484	1.330
		d	Å	4050	4060	4190	3870	→		2830	4960	4470	4000
		f	CPS	6460	6480	6670	6150	→		4510	7910	7120	6390
		t	MIN.	28.8	28.9	29.9	27.4	→		20.1	35.3	31.8	28.4
MONITOR RESISTORS	LOW Ω/SQ.	R´DESIGN	KΩ/SQ	1	1	5	1	1	5	1	0.1	1	–
		R´ACTUAL	↓	1.08	1.31	3.63	1.01	0.94	5.43	0.95	0.10	1.16	–
		L/W	SQ.	30.53	10.20	11.45	3.36	3.36	8.10	9.15	28.00	10.50	–
		R AT END OF OPERATION 2	KΩ	41.8	16.9	50.4	4.05	3.76	52.6	10.40	3.60	14.5	–
		R AT END OF OPERATION 3	↓	35.1	14.2	41.5	3.74	3.62	44.0	9.65	3.50	13.5	–
		R AT END OF OPERATION 4	↓	33.0	13.4	38.0	3.30	3.19	40.0	8.42	3.39	11.82	–
	HIGH Ω/SQ.	R´DESIGN	KΩ/SQ	–	–	–	10	10	–	10	10	10	5
		R´ACTUAL	↓	–	–	–	11.5	8.9	–	13.4	20.0	19.4	10.0
		L/W	SQ.	–	–	–	8.17	8.17	–	10.80	7.80	8.50	10.5
		R AT END OF OPERATION 5	KΩ	–	–	–	113	88.0	–	162	187	197	126
		R AT END OF OPERATION 6	↓	–	–	–	88	74.5	–	130	128	136	102
		R AT END OF OPERATION 7	↓	–	–	–	79	64.5	–	110	110	117	90

FOLDOUT FRAME

TABLE 3

PROCESS CHART - MELPAR MODEL I, THIN FILM CIRCUIT
MANUFACTURING FACILITY
CIRCUITS: R65018-1 and 5006-8 thru -16, except -14

NO.		OPERATION	MASK NO.	SOURCE MAT'L.	PRESSURE	SUBSTRATE HEAT		SOURCE HEAT				FILM THICK. MON.		FILM THICKNESS		RES. MON.	SHEET	DURATION
						E	T	E	I	P	T	df/dt	f	dd/dt	d	R	RES.@25°C	t
					TORR X 10^5	VOLTS	°C	KV	ma	WATTS	°C	CPS/MIN	CPS	Å/MIN.	Å	Ω	Ω/□	MIN.
1		DEPOSIT TERMINALS & TRIM BARS - FIRST LAYER	A	Cr	3 MAX.	2.5	200 ± 5	0.8	370	296 ± 5	1675	730	2050 ±10%	180	500	—	33	2.8
LOW Ω/SQ. OUTBOARD MON. L/W=	2	DEPOSIT INITIAL RESISTOR LAYER	B	Re*	↓	10.5	465* ± 5	4.76	150	713 ± 5	3320	—	—	~ 8	—	± 5%	—	2.6 TO 4.1 REF
	3	ANNEAL ABOVE	↓	↓	↓	↓	↓	—	—	—	—	—	—	—	—		—	10 ± 1
	4	DEP. & ANNEAL FINAL RESISTOR LAYER	↓	↓	↓	↓	↓	4.2	125	525 MAX	3100 MAX	—	—	~ 0.8 MAX	~ 21 TO 33	± 1%		10 ± 1
HIGH Ω/SQ. INBOARD MON. L/W=	5	DEPOSIT INITIAL RESISTOR LAYER	C	↓	↓	10	455 ± 5	4.76	150	713 ± 5	3320	—	—	~ 8	—	± 5%	—	2.4 TO 3.2 REF
	6	ANNEAL ABOVE	↓	↓	↓	↓	↓	—	—	—	—	—	—	—	—		—	10 ± 1
	7	DEP. & ANNEAL FINAL RESISTOR LAYER	↓	↓	↓	↓	↓	4.2	125	525 MAX	3100 MAX	—	—	~ 0.8 MAX	~ 19 TO 26	± 1%		10 ± 1
8		DEPOSIT TERMINALS & TRIM BARS - SECOND LAYER	A	Al NO. 1	↓	~ 0	85 ± 15	0.79	430	340 ± 5	1710	570	342 ±10%	366	220	—	1.5/3.0	0.6
9		DEPOSIT LOWER CAP. PLATES & CONDUCTORS	D	↓	↓	↓	70 ± 5	↓	↓	↓	↓	↓	3420 ± 10%	↓	2200	—	0.15/0.30	6
10		ANNEAL ABOVE	↓	—	↓	3.5	300 ± 5	—	—	—	—	—	—	—	—	—	—	10 ± 1
11		DEPOSIT CAPACITOR DIELECTRIC	E	$SiO + B_2O_3$	4 TO 5 O_2 BLEED	2.5	200 ± 5	0.635	300	190 ± 5	1495	452 INITIAL		284* INITIAL		—	—	UNTIL df/dt <70 (MIN)
12		DEPOSIT UPPER CAP. PLATES & CONDUCTORS	F	Al NO. 2	3 MAX.	~ 0	70 ± 5	0.79	430	340 ±5	1710	570	3420 ±10%	366	2200	—	0.15/0.30	6
13		DEPOSIT RESISTOR PROTECTIVE COAT	G	SiO	↓	2.5	200 ± 5	0.58	210	122 ± 5	1350	454	2270 ±10%	400	2000	—	—	5

NOTES FOR TABLE 3

1. The following may be determined from Table 2.

(a) Mask Numbers

(b) Quantity of B_2O_3 + SiO mix to load in capacitor dielectric source prior to each batch. This is specified as M grams ± 1% and shall consist of 70% SiO + 30% B_2O_3 by weight.

(c) "Film Thickness Monitor" frequency change f, film thickness, d, deposition time, t, and capacitance per unit area, C/A, for the capacitor dielectric deposition.

(d) Final sheet resistance, $R^{\square}$; length to width ratio, L/W; and resistance, R, for the monitor resistors. Cutoff values for the low (operations 2, 3, and 4) and high (operations 5, 6, and 7) sheet resistance depositions are given.

2. For circuits R65018-1 and 5006-8, substrate temperature shall equal 460 ± 5°C during operation 2 and 500 ± 5°C during operations 3 and 4. (This reduces the TCR at the expense of a somewhat reduced yield.)

3. Source power listed for Re is for a maximum size Re slug of 25.76 grams. For smaller slugs, reduce power in accordance with Figure 23.

4. Prior to each batch, load 0.3 grams ± 10% of aluminum in each aluminum source.

5. For circuits having large capacitance area, such as 5006-13 and -15, the number of capacitors having shorted plates can be reduced by purging the vacuum system with argon or air between steps 7 and 8. This appears to result in smoother aluminum capacitor

plates. It is hypothesized that the purge removes hydrogen released during chromium evaporations and that hydrogen promotes grain growth in aluminum films. In any event, aluminum films deposited after chromium evaporations, without an intervening purge, are usually rougher, which leads to a greater number of shorted capacitors.

6. Post Vacuum Capacitor Treatment:

The following procedure is recommended for eliminating short circuits and improving the dielectric strength, dissipation factor, moisture resistance, and life of capacitors and crossovers.

(a) Apply 3 Vdc across each capacitor for 1 to 2 seconds. This eliminates most shorts resulting from small particles, pinholes, or a rough, grainy structure in the lower initially deposited plate.

(b) Check dc resistance of all capacitors, at 1.5 Vdc. This is the voltage typically applied by a VTVM when set at its maximum resistance range. For those capacitors having less than 10 megohms resistance, apply voltage pulses at progressively higher amplitudes, starting at 5 volts, until the resistance is greater than 10 megohms or the amplitude equals 20 volts.

(c) Complete oxidation of capacitor dielectric (in case it was not completely oxidized during deposition) and drive moisture from capacitors by heating in an air oven at 100 $\pm$ 5^{o}C for 1 to 2 hours.

(d) Immediately after removing the substrates from the oven, apply a 1 to 4 mil thick protective coating of "Humeseal 1H34". This coating affords good moisture and abrasion protection and is rated for use up to 200°C. It can be applied by dipping or spraying but is normally applied by brushing on with a small paint brush to avoid coating of solder terminals. The substrates must be maintained at a temperature of 40 to 100°C until after the coating is applied to minimize moisture absorption. This can be accomplished with a heat lamp.

(e) Repeat step (b), except the resistance must be greater than 1000 megohms at 1.5 Vdc. Reject all circuits containing capacitors that fail to meet this requirement.

NOTE: When attempts are made to repair shorted capacitors by applying voltage across the capacitor care must be taken to prevent parallel resistors from burning out. Also, when capacitors are in parallel with resistors, the D.C. resistance measurement shall be equal to or greater than the minimum allowable value for the resistor.

FOLDOUT FRAME

FOLDOUT FRAME

TABLE 4

PROCESS CHART - MELPAR MODEL I, THIN FILM CIRCUIT
MANUFACTURING FACILITY
CIRCUIT: 5006-14 UNIVERSAL RF AMPLIFIER

NO.		OPERATION	MASK NO.	SOURCE MAT'L.	PRESSURE	SUBSTRATE HEAT E	SUBSTRATE HEAT T	SOURCE HEAT E	SOURCE HEAT I	SOURCE HEAT P	SOURCE HEAT T	FILM THICK. MON. df/dt	FILM THICK. MON. f END	FILM THICKNESS dd/dt	FILM THICKNESS d	RES. MON R END	SHEET RES. @ 25°C	DURATION t
					TORR X 10^{-5}	VOLTS	°C	KV	ma	WATTS	°C	CPS/MIN	CPS	Å/MIN	Å	Ω	Ω/□	MIN.
1		DEPOSIT TERMINALS FIRST LAYER	7	Cr	3 MAX.	2.5	200 ± 5	0.8	370	296 ± 5	1675	730	2050 ± 10%	180	500	—	33	2.8
LOW Ω/SQ. OUTBOARD MON. L/W = 28	2	DEPOSIT INITIAL RESISTOR LAYER	2	Re*		10	460 ± 5	4.76	150	713 ± 5	3320	—	—	~ 8	—	3.6 K ± 5%	—	15
	3	ANNEAL ABOVE	↓	↓		12	500 ± 5	—	—	—	—	—	—	—	—	3.5 K ± 1%	—	10 ± 1
	4	DEP. & ANNEAL FINAL RESISTOR LAYER	↓	↓		↓	↓	4.4	132	580 MAX	3200	—	—	~ 1.6 TO 0	~ 128	3.39 K ± 5%	100	10 ± 1
HIGH Ω/SQ. INBOARD MON. L/W = 7.8	5	DEPOSIT INITIAL RESISTOR LAYER	3	↓		10	460 ± 5	4.76	150	713 ± 5	3320	—	—	~ 8	—	187 ± 5%	—	2.4
	6	ANNEAL ABOVE	↓	↓		↓	↓	—	—	—	—	—	—	—	—	128 K ± 1%	—	10 ± 1
	7	DEP. & ANNEAL FINAL RESISTOR LAYER	↓	↓		↓	↓	4.2	125	525 MAX	3100	—	—	~ 0.8 TO 0	~ 19	110 K ± 1%	20 K	10 ± 1
8		DEPOSIT TERMINALS - SECOND LAYER	7	Cr		2.5	200 ± 5	1	400	400 ± 5	1820	1025	2050 ± 10%	250	500	—	20	2
9		DEPOSIT TERMINALS - THIRD LAYER	↓	Cu		3.5	300 ± 5	0.77	260	200 ± 5	1510	954	10,000 ± 10%	182	1910	—	0.1	10.5
10		DEP. LARGE CAPACITOR PLATES & SOME RES. TERMINALS & CONDUCTORS	5	Al NO. 1		~ 0	70 ± 5	0.79	430	340 ± 5	1710	570	5120 + 10% − 0	366	3300	—	0.1/0.2	9
11		ANNEAL ABOVE	↓	—	↓	3.5	300 ± 5	—	—	—	—	—	—	—	—	—	—	10 ± 1
12		DEPOSIT CAPACITOR DIELECTRIC	4	$SiO + B_2O_3$	4 TO 5 O_2 BLEED	2.5	200 ± 5	0.635	300	190 ± 5	1495	452 INITIAL	7910	284* INITIAL	4960	—	—	UNTIL df/dt ≤ 70 (36 MIN)
13		DEP. SMALL CAP. PLATES, TRIM BARS, & REMAINING RES. TERM. & CONDUCTORS	1	Al NO. 2	3 MAX.	~ 0	70 ± 5	0.79	430	340 ± 5	1710	570	5120 + 10% − 0	366	3300	—	0.1/0.2	9
14		ANNEAL & OXIDIZE DIELECTRIC	—	—	1 ATM. AIR	—	25 ± 5	—	—	—	—	—	—	—	—	—	—	90 ± 15
15		DEPOSIT RESISTOR PROTECTIVE COAT	6	SiO	3 MAX.	2.5	200 ± 5	0.58	210	122 ± 5	1350	454	2270 ± 10%	400	2000	—	—	5
16		DEPOSIT CAPACITOR PROTECTIVE COAT	4	↓	↓	↓	↓	0.5	200	100 ± 5	1300	245	↓	215	↓	—	—	9.3

NOTES:

1. PRIOR TO EACH BATCH, LOAD 1.65 ± 0.01 GM. OF BOROSILICATE MIX IN CAPACITOR DIELECTRIC CRUCIBLE. MIXTURE SHALL CONSIST OF 70% SiO + 30% B_2O_3 BY WEIGHT.
2. CAPACITANCE/UNIT AREA = 50,000 PF/SQ. IN.
3. PRIOR TO EACH BATCH, LOAD 0.4 GM ± 10% OF ALUMINUM IN EACH Al SOURCE.
4. PURGE VACUUM CHAMBER WITH ARGON BETWEEN STEPS 9 & 10.
5. DURING STEP 14, INSTALL SiO CRUCIBLE IN PLACE OF BOROSILICATE CRUCIBLE.
6. SOURCE POWER LISTED FOR Re IS FOR A MAX. SIZE Re SLUG OF 25.76 GM. FOR SMALLER SLUGS, REDUCE POWER IN ACCORDANCE WITH FIGURE 1.
7. REMOVE DISKS FROM SUBSTRATE PALLET.

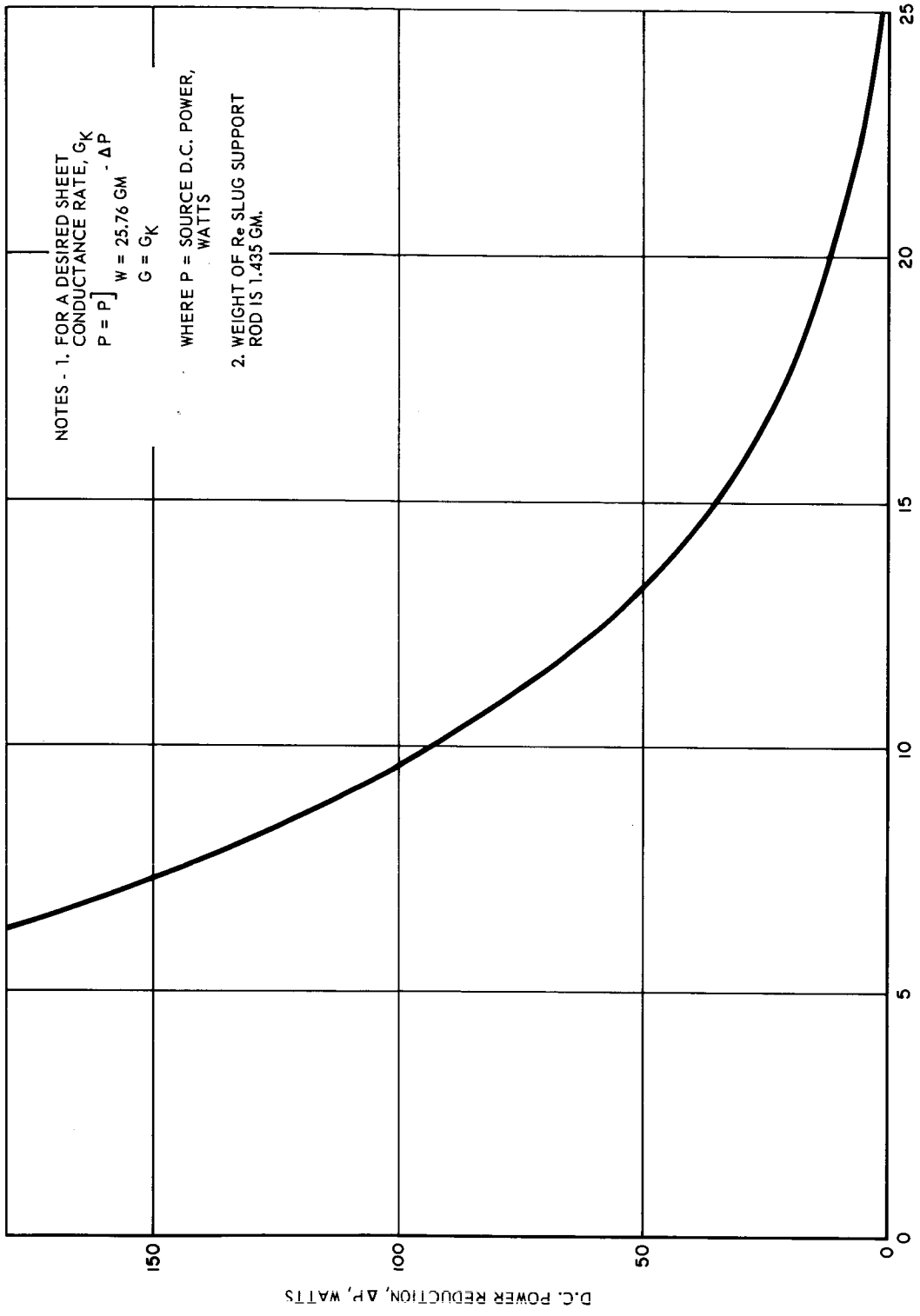


Figure 33. DC Power Reduction vs. Size of Re Slug

APPENDIX A-2

Circuit Assembly Procedure

a. Scribe and dice the substrates into individual circuits, as required.

b. Trim all capacitors and certain resistors to specified values. For RF circuits, all resistors are trimmed to their final values at this point.

c. Blow off glass chips with a gentle flow of clean, dry gas.

d. Tin all solder pads, pins, and non-gold leads of discrete components. Thoroughly remove varnish from coil leads before soldering. Use a hydrazine activated flux, Fairmont H100, and a relatively large soldering iron for tinning wires. Make sure the leads are completely coated with solder.

e. Solder circuit pins using a jig to hold the pins in their proper positions. All pins consist of .018 to 0.020 inch diameter x 0.500 inch long phosphor-bronze or gold-plated kovar and are soldered to 0.040 inch wide x 0.125 inch long thin-film terminals located on 0.075 inch centers along one edge of the substrate. Distance between pins is controlled to an accuracy of $\pm$ 5 mils by the jig. For RF circuits, pin no. 1 must be .080 $\pm$ .005 inch from the left edge of the substrate.

f. Fasten discrete components and reinforce pins using non-conducting epoxy cement. Prevent epoxy from coating capacitors, solder pads, or ends of leads. Cure epoxy in oven at 60°C for 30 minutes.

g. Solder all discrete component leads.

h. Test circuit and adjust as required. For most circuits, several of the resistors are trimmed to obtain specified voltages in this step. For RF circuits, the variables discrete capacitors are adjusted to obtain peak voltage gain.

i. Store circuits in clean, dry container.

NOTES:

1. For Cr-Al thin film terminals, the solder shall consist of 65% tin, 25% bismuth, and 10% silver. The soldering iron should be at a temperature of 260°C. Wire leads must be tinned with the same

solder. Resin flux may not be used. After soldering, the circuits should not be heated above 125°C, as the Al films may dissolve into the solder, causing open circuits.

2. For Cr-Cu terminals, use standard resin core, lead-tin solder. The soldering iron should be just hot enough to melt the solder.

3. For RF circuits, spotweld a 5 mil dia. gold jumper wire from terminal 2 to the nearest dielectric free point on the Al conductor leading from terminal 2 to C4a (between C4a and C4b). Use three low power pulses to weld the gold lead at each end. Power should be just barely high enough to make the wire "stick" after the first pulse. Inspect the opposite side of the Al film after welding; gold shall not be visible. Welding is accomplished with a split-tip, parallel resistance microbond welder, Weldmatic Model 1090C. The above low power multiple pulse technique produces strong joints without fracturing the glass because thermal shock is reduced.

4. After RF circuits are assembled, they are fastened to a brass base using epoxy cement. They are precisely located by means of a jig, Sketch T-2. The base is placed on the jig and pressed against the large pins, with the small pins protruding through holes in the base. The proper RF circuits are then coated with epoxy on the non-film side and cemented to the base. The left edge of the substrate is pressed against two small pins and the terminal edge is pressed against the adjacent portion of the base. The lower surface of the substrate must be in contact with the base, except for the 1 to 2 mil thick epoxy coating. The epoxy cures within 24 hours at 25°C or within 30 minutes at 60°C. The epoxy may be softened and the substrate removed by heating the brass base with a soldering iron.

5. Use the following active devices for all circuits, except RF circuits:

Transistors - 2N3071 (chip form)
Diodes - HMG9007

Transistor Chip Preparation

Chip transistors are used for all circuits except for some of the RF circuits for which transistors are available in cans only. Chip size is 20 mils x 30 mils x approximately 3 mils thick. The chips are prepared as follows:

a. Spot-weld a 50-mil-diameter x 5-mil-thick gold plated kovar disk to a TO 5 transistor header.

b. Place a transistor chip on the above disk with two 15-mil-diameter x 1-mil-thick gold-silicon preforms (manufactured by Corning Corp. of America) sandwiched between the chip and disk. The gate side of the chip must face the preform.

c. Heat the header on a hot plate (containing an access hole for the header leads) at 410°C to 420°C for about 5 minutes. This melts the preform and bonds the chip to the disk. The chip must be agitated in order to form a good bond. This is probably necessary in order to break through a thin oxide or slag at the surface of the molten preform so that the preform material may wet the silicon. Agitation is accomplished by hand using a vacuum needle to grasp the chip.

d. Fasten 1-mil-diameter gold wires between the source and drain terminals of the chip and the source and drain pins of the header, using thermocompression, ball bonding.

e. Fasten a 5-mil-diameter gold lead between the disk and the gate pin of the header using a split-tip resistance welder.

f. Test the device on a curve tracer. Approximately 15% of the transistors are rejected at this point.

g. Remove the device from the header. This is done by breaking the spot-weld between the kovar disk and the header and by cutting the leads at the header pins using a small knife.

h. Store in a clean, dry container.

APPENDIX B

TEST PROCEDURE FOR RECEIVER, SIMPLEX AND DUPLEX MODES

Sensitivity, AGC, IF Bandwidth and Operating Frequency

1. Assemble input setup consisting of Hewlett-Packard (H.P.) 608D signal generator, H.P. 650A audio oscillator, Narda 3000-20 directional coupler and H.P. 524B - H.P. 525C counter-converter combination. Use H.P. 650A to externally modulate H.P. 608D. Use directional coupler to sample IF power for frequency measurement.

2. Assemble output setup consisting of Tektronix 535A oscilloscope with 53B plug in unit. A 600 ohm resistor must be placed across the oscilloscope input to load the transceiver properly.

3. Connect input setup directly to the transceiver rf antenna connector and adjust the 608D generator for an output frequency of 259.7 mHz at an amplitude of 7 microvolts. Modulation should be 1000 cycle sine wave at 30% amplitude.

4. Make sure that transceiver gain is set at maximum and connect output setup directly to the audio channel.

5. Energize transceiver at nominal voltage, measure and record the peak amplitude of the signal plus noise and also the trace width due to noise. Trace width should be no more than 50% of the peak amplitude recorded.

6. Increase rf input signal to 0.4 volts, measure and record peak amplitude of the 1000 cycle output signal. Peak should be at least 4.25 volts, but less than 3.16 times the peak signal amplitude recorded in step 5, allowing for trace width.

7. Reduce the rf input signal to a more convenient level, measure and record the peak amplitude of the 1000 cycle signal.

8. Increase rf input signal by 3 DB and increase the rf frequency until the 1000 cycle peak amplitude returns to the value recorded in step 7. Switch off modulation temporarily, measure and record the rf frequency.

9. Without changing rf level from that set in step 8, switch on modulation and reduce the rf frequency until the 1000 cycle peak amplitude returns to the value recorded in step 7. Switch off modulation temporarily, measure and record the rf frequency.

10. The rf frequencies measured in steps 8 and 9 should differ by at least 70 KHz and should have approximately symmetrical spacing about 259.7 mHz.

TEST PROCEDURE FOR TRANSMITTER, SIMPLEX MODE

A. VOX, Carrier Power, Frequency and Frequency Stability

1. Set up transceiver for simplex mode with provision for audio input and place a 20 DB pad between the rf antenna connector and a Hewlett-Packard (H.P.) 477B thermistor and H.P. 430C power meter setup.

2. Prepare to supply the transceiver audio input with a 1000 cycle signal at 1 mv rms amplitude. The setup required consists of a H.P. 650A and 600 ohm load resistor. Switch off audio signal before energizing transceiver.

3. Energize transceiver at nominal supply voltage and observe the H.P. 430C power meter. There should be no carrier output because of the VOX circuit.

4. Switch on the 1 mv audio signal and observe the power meter. It should rise immediately to an average modulated level of approximately 225 mw. Record the reading obtained.

5. Switch off the audio signal. The power should drop to approximately 150 mw and remain at that level for approximately 2 seconds before shutting off. Record the reading obtained.

6. Leaving the transceiver energized and the 20 db pad in place, replace the thermistor mount with a 50 ohm cable to a H.P. 524B--H. P. 525C counter-converter setup.

7. Apply the audio signal just long enough to switch the VOX and then measure and record the transceiver frequency during the 2 second unmodulated carrier interval.

8. Repeat step 7 except maintain the audio signal for approximately 5 minutes. Both measurements should be within $\pm$ .005% of 296.8 mHz.

B. Voice Modulation Percentage and Frequency Response

1. Set up transceiver as in part A with the audio oscillator and load resistor connected to the audio input. Place a 10 db pad between the rf antenna connector and a H.P. 420A crystal detector.

2. Feed the detector output into a H.P. 302A wave analyzer by means of a 15K load resistor and 0.05 mf coupling capacitor.

3. Energize transceiver and apply a 250 cycle, 1 mv rms signal to the audio input.

4. Measure and record the rms amplitude of the 250 cycle signal appearing at the detector output. Using a H.P. 410B VTVM, measure and record the D.C. voltage across the detector load resistor.

5. Repeat step 4 for frequencies of 1000 and 3000 cycles. Rms amplitudes of the detector output signals for all three frequencies should be approximately equal. Peak amplitudes for the three signals should approximate 95% of the dc detector voltages measured.

6. Reset the audio oscillator to a frequency of 4.6 kHZ and adjust for a 1 mv rms signal into the audio channel.

7. Measure and record the rms amplitude of the 4.6 kHz signal present at the detector output. It should be no greater than 6.3% of the 1000 cycle rms amplitude measured in step 5.

TEST PROCEDURE FOR TRANSMITTER, DUPLEX MODE

A. Carrier Power, Frequency and Frequency Stability

1. Set up transceiver for duplex mode with no data or voice input and place a 20 db pad between the rf antenna connector and a Hewlett-Packard (H.P.) 477B thermistor and H.P. 430C power meter setup.

2. Energize transceiver at nominal supply voltage and measure and record the output power. A minimum output of 150 mw should be observed.

3. Leaving the transceiver energized and the 20 db pad in place, replace the thermistor mount with a 50 ohm cable to a H.P. 524B - H.P. 525C counter-converter setup. Measure and record the transceiver frequency.

4. Shut off transceiver power for a minimum period of 5 minutes and repeat the frequency measurement immediately after the transceiver is reenergized. Both measurements should be within $\pm$ .005% of 296.8 mHz.

B. Telemetry Modulation and Overall Frequency Response

1. Set up transceiver for duplex mode with no data or voice inputs and a 10 db pad between the rf antenna connector and a H.P. 420A crystal detector.

2. Feed the detector output into a H.P. 302A wave analyzer by means of a 15K load resistor and 0.05 mf coupling capacitor. Feed the analyzer frequency restorer output into a H.P. 524B counter.

3. Energize transceiver, measure and record both the frequencies and rms amplitudes of the 7 telemetry signals present in the detector output. Using a H.P. 410B VTVM, measure and record the dc voltage across the detector load resistor.

4. Peak amplitudes (1.41 x rms) of the 7 telemetry signals should be approximately equal and each should be approximately 10.7% of the dc voltage recorded in step 3.

NOTE: It is assumed that the data response of the channels will be measured on the NASA setup. Otherwise, the present arrangement may be employed in conjunction with accurately known D.C. voltages applied to the telemetry inputs.

C. Voice Modulator Sensitivity and Filter Response

1. Use setup identical with that of part B, except provision is made for input to the voice channel.

2. With a H.P. 650A audio oscillator, and 600 ohm load resistor, apply 1 mv rms at 1000 cycles to the audio input.

3. Repeat step 3 of part B, except that the 1000 cycle rms amplitude and the dc voltage level are the only values measured and recorded.

4. The peak amplitude of the 1000 cycle signal should be approximately 20% of the dc voltage level recorded in step 3.

5. Reset the audio oscillator to a frequency of 4.6 kHz and adjust the output for 1 mv rms into the audio channel.

6. Measure and record the rms detector output voltage at 4.6 kHz. It should be no greater than approximately 6.3% of the 1000 cycle rms amplitude recorded in step 3.